Digital Equipment Corporation
Maynard, Massachusetts

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PDP-10
MA10 Core Memory
Maintenance Manual
Volume I

DEC-10-HIAA-D

PDP-10
MA10 CORE MEMORY MAINTENANCE MANUAL VOLUME I

DIGITAL EQUIPMENT CORPORATION ▫ MAYNARD, MASSACHUSETTS

1st Printing September 1969

Instruction times, operating speeds and the like are included in this manual for reference only; they are not to be taken as specifications.

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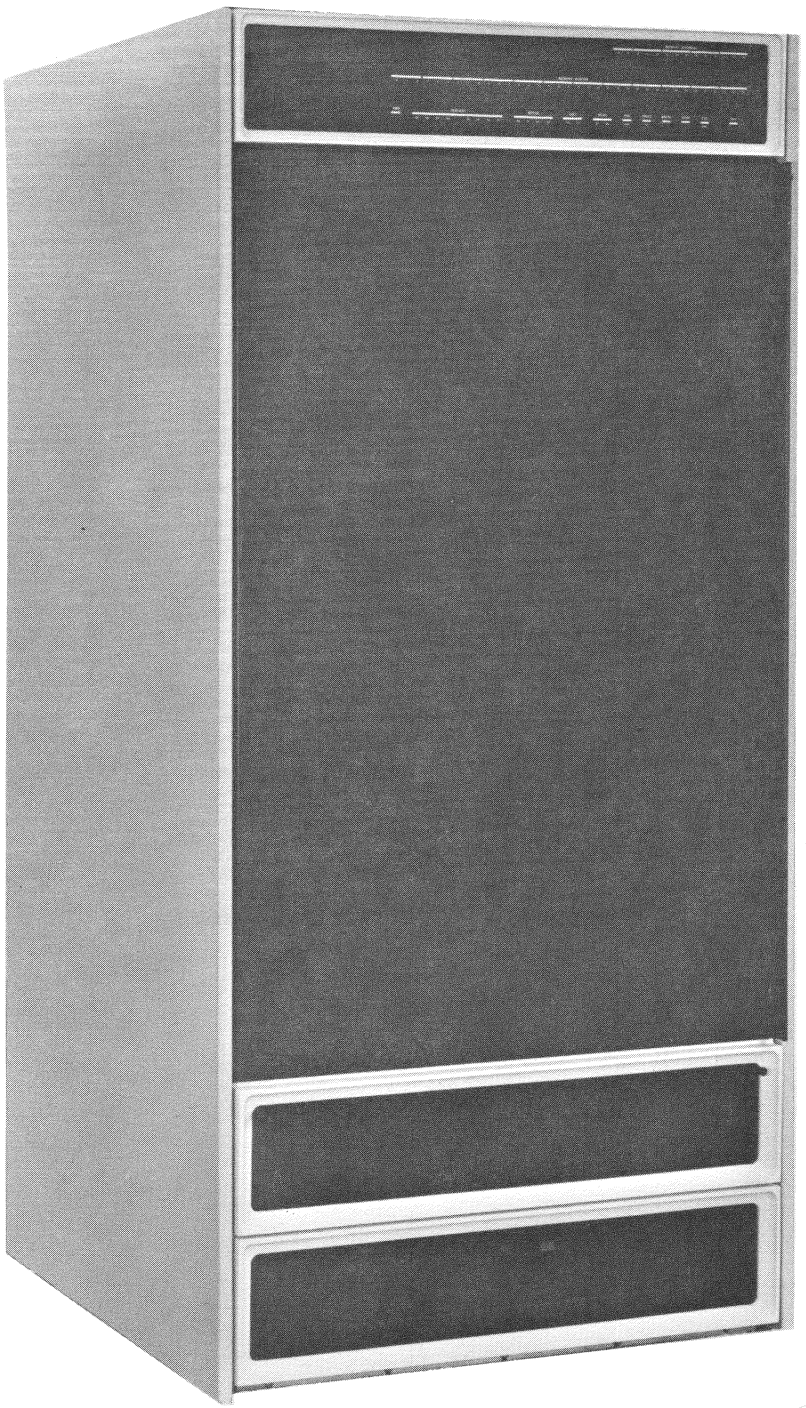

MA10 Core Memory

CHAPTER 1
GENERAL INFORMATION

1.1 SCOPE

This manual, in two volumes, presents the information necessary for the installation, operation, and maintenance of the MA10 and MA10A Core Memories which are manufactured by Digital Equipment Corporation and are intended for use with the DEC PDP-10 Digital Computer.

Reference documents which contain information supplementing that contained in this manual are listed in Section 1.6. Volume II contains the MA10/MA10A Engineering Drawings.

1.2 GENERAL DESCRIPTION

The MA10 and MA10A are ferrite core memory units possessing 930 ns cycle times. Stack arrangement is of the 2-1/2 D, 3-wire type which allows for storage of 37-bit words (36-bits and parity). The two units differ only in their storage capacities (the MA10 stores 16,384 words and the MA10A stores 8,192 words), and each is housed in a standard PDP-10 cabinet. A maximum of 16 of either memory type (262,144 word capacity if all are MA10s) may compose a single system.

Operation within the PDP-10 computer system is asynchronous; access to memory units is governed by a "Request-Response" system wherein the processor makes a request and waits for a response from a memory unit. Figure 1-1 illustrates the information transfer between the processor and the memory unit.

Since up to 16 memory units may be included within a system, information contained in the memory address word (MADR bits 18 through 21) is used to select the desired unit. Settings of the MADR bit 18 through 21 switches, located on the memory unit switch panels, determine which memory unit will respond when addressed.

A memory unit may contain up to four access ports; each port is associated with one particular processor, data channel, multiplexor, DA Interface, etc. If an MX10 Memory Data Multiplexor is included in the system, as many as eight DF10 Data Channels may be associated with one memory port. Priority network logic contained within each memory unit designates the sequence of processor access in the event of simultaneous requests.

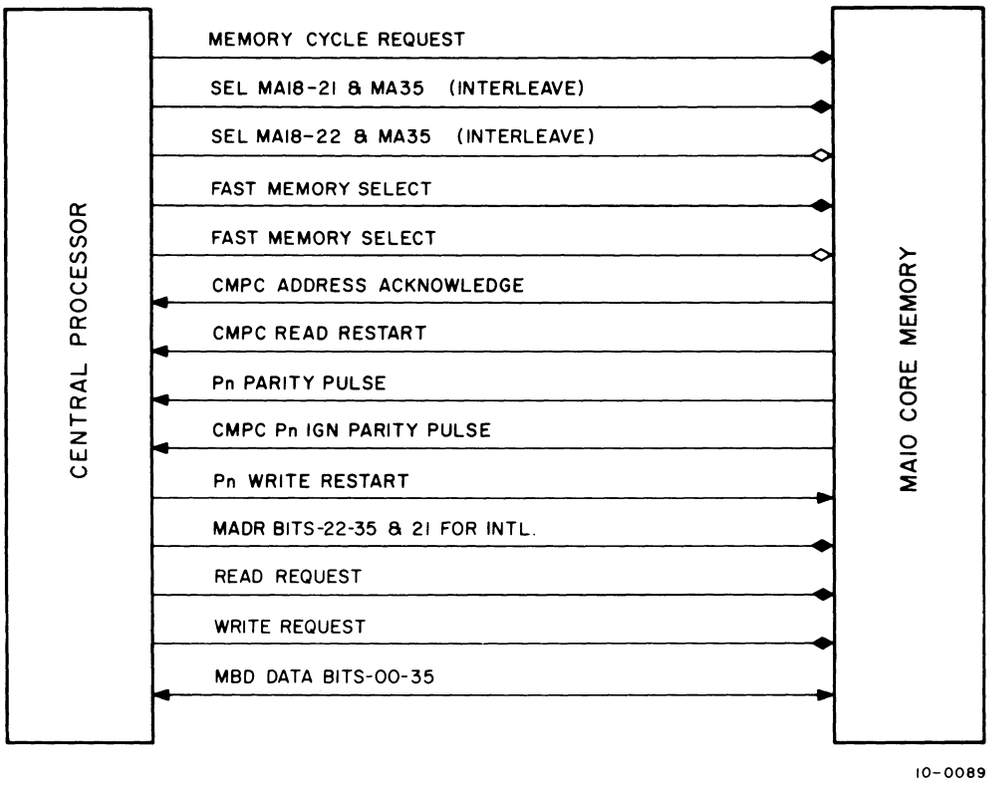

Figure 1-1 Memory-Processor Interface

Systems containing more than one memory unit (MA10 only) may be operated in an interleaved memory-cycle mode through manipulation of the Interleave Switches located on the memory unit switch panels. Interleaving alternates successive memory cycles between a pair of memory units if the addressing sequence refers to successive memory locations. Operation in this mode effectively decreases cycle time which, in turn, reduces processor idle time.

Communication between processor and memory unit takes place over the memory bus which consists of two coaxial cable assemblies. Each processor in the system has an associated memory bus which is connected to an active port in each memory unit. Figure 1-2 is a typical system interface diagram. The maximum length of the memory bus must not exceed 100 ft including equipment interior wiring.

Figure 1-3 is a front view of the MA10 with the door removed; Figure 1-4 illustrates the rear plenum door.

1.2.1 Control Logic

Each MA10/MA10A contains the following major sections of logic:

a. Core Memory Address (CMA)
b. Core Memory Address Buffers (CMAB)
c. Core Memory Buffer (CMB)
d. Core Memory Control (CMC)

e. Core Memory Digit Selectors (CMDS)
f. Core Memory Processor Control (CMPC)
g. Core Memory Sense Control (CMSC)
h. Core Memory Word Selection (CMWS)
i. Core Memory Power Regulation (CMPR)

Storage and retrieval of data within the memory unit is controlled by processor request signals, processor data, and pulses and levels generated in the CMC and CMPC logic.

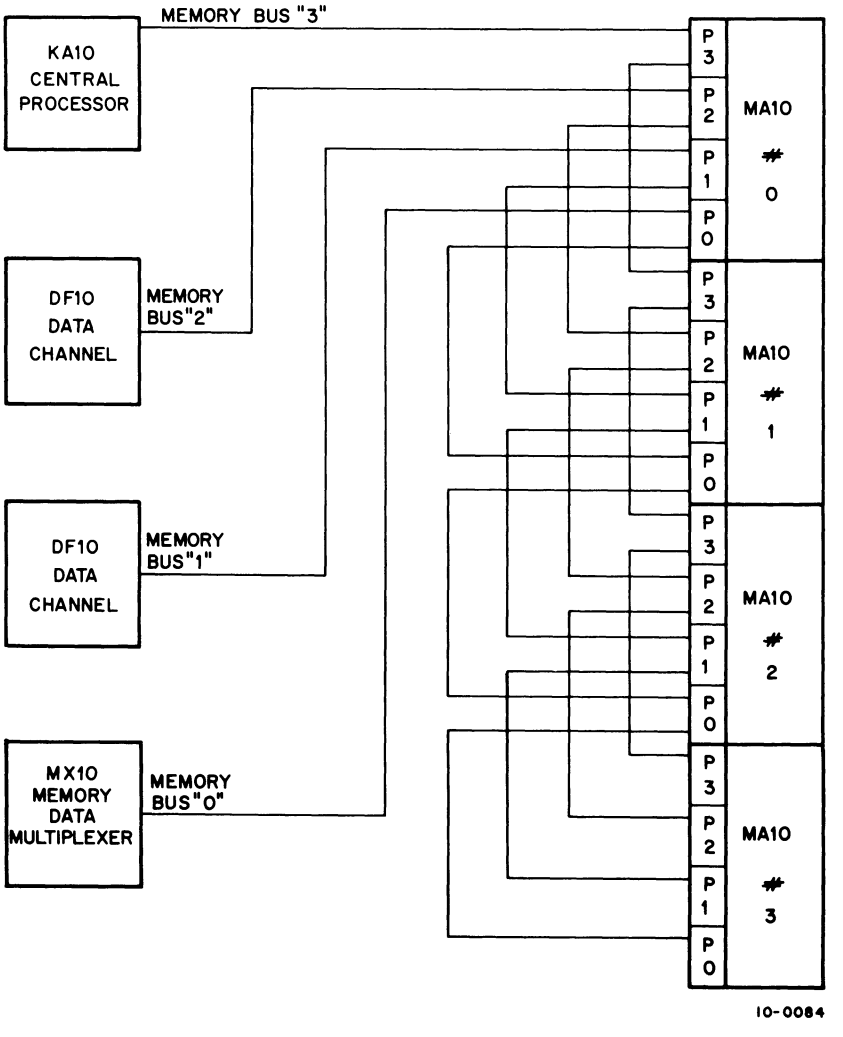

Figure 1-2 System Interface

Odd parity is generated in the processor and is transmitted to the memory over the parity pulse line. Parity is not checked in the memory unit; it is stored with the data and transmitted to the processor with the associated data word.

If the memory does not have provisions for storing and transferring parity information (only true for the MA10/ MA10A when the parity bit circuitry has been substituted for a data bit as in the case of a temporary maintenance procedure), the memory unit sends the IGN PARITY pulse to the processor simultaneously with ADDR-ACK.

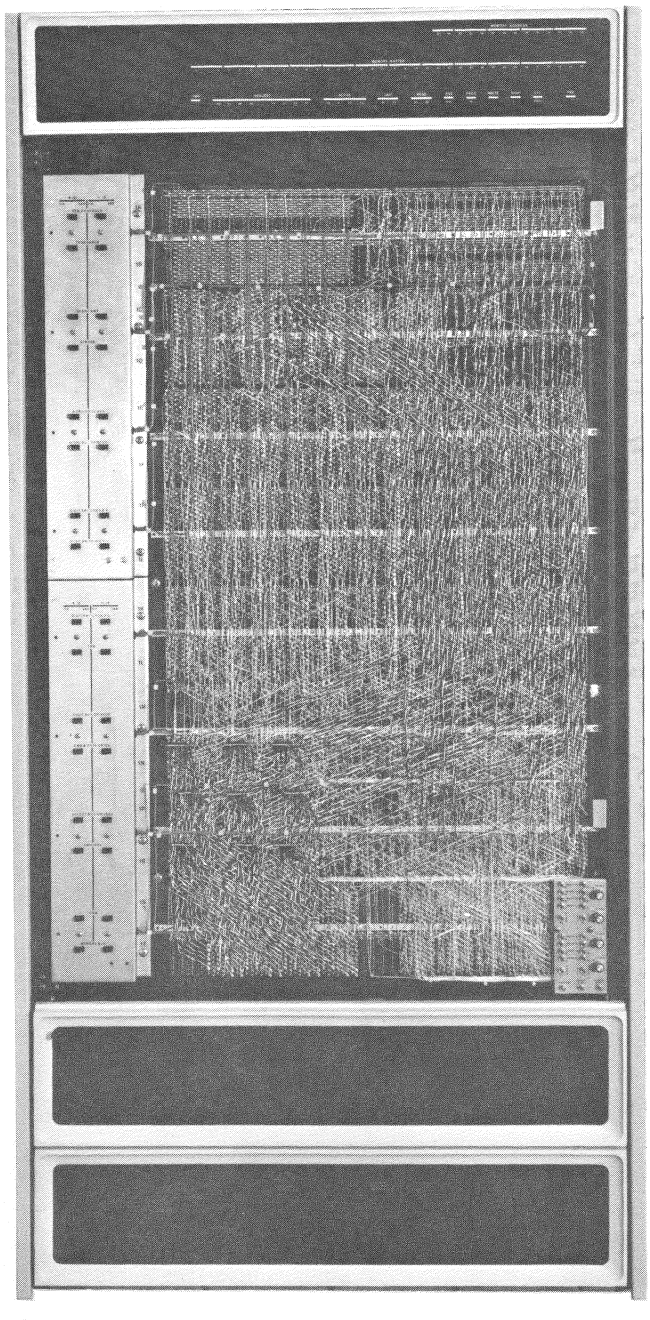

Figure 1-3 MA10 Front View (Door Removed)

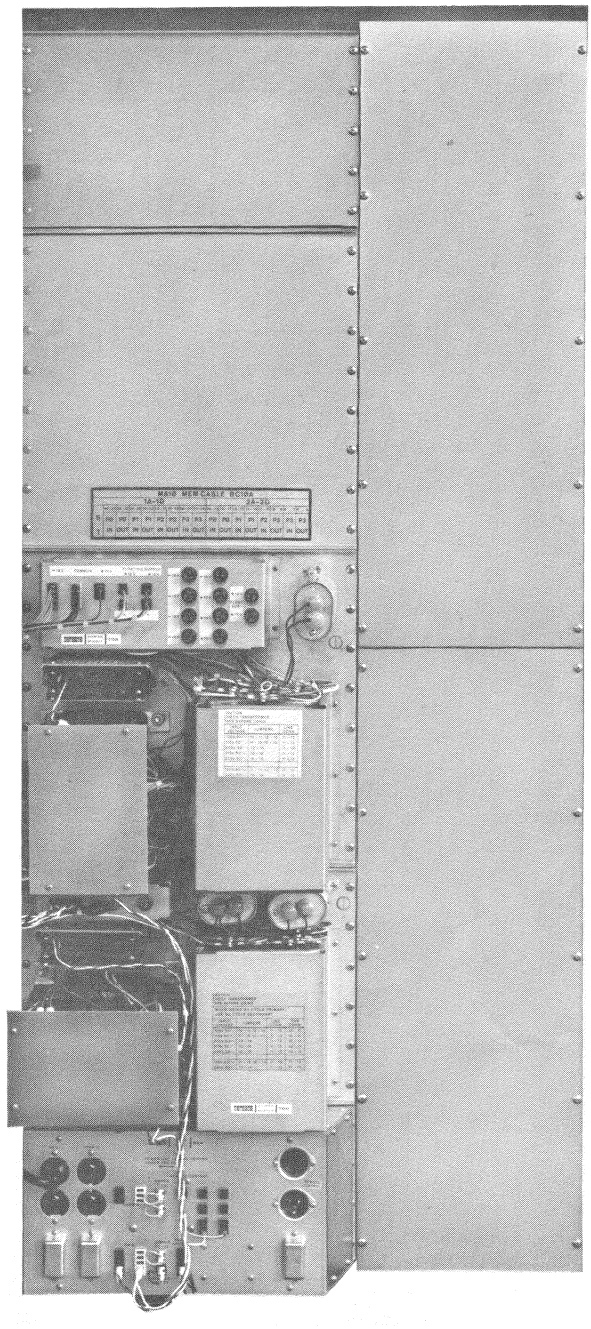

Figure 1-4 MA10 Plenum Door

The CMA receives, over the MADR lines, information from the processor which determines the location of the data to be written into or read out of the stack and the type of memory cycle request being made (read, write, or read-modify-write).

Data to be written into the stack is placed on the memory bus by the processor, temporarily stored in the MB, and then is written into the stack through the MB. During the restore portion of a read-restore cycle, the data read from the selected address and stored in the MB is written back into the selected address.

Retrieval of data from the memory stack is accomplished by sense field selection; the memory location is read and the data sensed is applied to the sense amplifiers whose outputs are strobed to the memory bus and the MB.

1.2.2 Stack

The memory stack is constructed of coincident current ferrite core arrays in a 2-1/2D, 3-wire configuration. In this type of organization, the read portion of the memory cycle is similar to that of a 4-wire, 3D memory in that half-read currents in both X (word) and Y (digit) lines result in the core at the intersection of these lines being subject to a full read current. If a 1 is to be written, both digit and word currents are turned on. However, if a 0 is to be written, the digit half-write current is not turned on and thus only word current is supplied. Therefore, in a 2-1/2D system, the inhibit windings such as exist in a 3D memory are not necessary. Appendix C contains a discussion of core memory fundamentals.

1.3 SPECIFICATIONS

Table 1-1 lists the specifications for the MA10 and MA10A. Cabling information is contained in the Installation Section, Chapter 2.

Table 1-1
Specifications

Characteristic	Specification
Power Requirements: (The equipment will operate with any of the indicated combinations after appropriate internal power supply and control adjustments are accomplished).	110 Vac 50 Hz 115 Vac 50 Hz 200 Vac 50 Hz 215 Vac 50 Hz 230 Vac 50 Hz 120 Vac 60 Hz 240 Vac 60 Hz
Line Current (Steady State at 120 Vac)	20A
Line Current (Surge at 120 Vac)	40A (One Second Duration)
Power Dissipation	1600 W
Internal Logic Potentials	+10V, -15V
Power Interrupt	Up to 25 ms with no effect on operation. No loss of stored data at power ON or OFF.

Table 1-1 (Cont)
Specifications

Characteristic	Specification
Cycle Time	930 ns maximum
Read Access Time	550 ns maximum (serial numbers 1, 2, 60 and beyond) 580 ns maximum (serial numbers 3-59)
Address Acknowledge Time	200 ns maximum
Word Length	36-bit plus parity
Memory Size	
MA10	16,384 words
MA10A	8,192 words
Access Ports	Four
Dimensions	
Height	69 in. (1753mm)
Width	32-1/2 in. (826mm)
Depth	27 in. (686mm)
Weight	750 lb. (340.2 kg)
Operating Temperature	60°F to 95°F (15.6°C to 35°C)
Storage Temperature	40°F to 110°F (4.4°C to 43.3°C)
Relative Humidity	20% to 80%
Maximum Wet Bulb	78°F
Heat Dissipation	5440 BTU/hr

1.4 MODULE UTILIZATION

DEC Type No.	Function	DEC Type No.	Function
B133	Diode Gate	G023	Master Slice Control
B134	Diode Gate	G217	Memory Word Driver
B135	Diode Gate	G219	Memory Selector (Rev. E or beyond)
B136	Diode Gate	G626	Resistor Board (with fuse)
B137	Diode Gate	G700	100Ω Terminator
B165	Inverter	G703	100Ω Bus Terminator
B169	Inverter	G704	2mA Level Terminator
B172	Diode Gate	G805	Negative Regulator (Rev. D or beyond)
B212	Dual R-S Flip-Flop	G810	6V Regulator Control
B214	Quadruple Flip-Flop	G816	Regulator Control
B311	Tapped Delay Line	M502	Negative Input Converter
B312	Delay	R002	Diode Cluster
B611	Pulse Amplifier	R303	Integrating One Shot
B685	Diode Gate Driver	W010	Clamped Load
G022	Four Input Sense Amplifiers	W102	Pulsed Bus Transciever (Rev. H or beyond)
		W501	Schmitt Trigger

1.5 MNEMONICS

Appendix A is a Glossary of the mnemonics which appear in this manual and on the engineering drawings which accompany the equipment. Levels and pulses are logically designated according to the logic section in which they are developed; i.e., CMA CLR is developed in the Core Memory Address logic.

1.6 OPTIONAL ACCESS PORTS (MC10)

Each memory unit is supplied to the user with one set of the cables required for connection to a processor or to another memory unit through one port. For each additional port activated (up to a total of four), one MC10 option must be procured.

1.7 REFERENCE DOCUMENTS

The following documents supplement the information contained in this manual:

PDP-10 System Reference Manual

KA10 Central Processor Maintenance Manual

PDP-10 Installation Manual

PDP-10 Interface Manual

This material is available from the nearest DEC Field Office or from:

Digital Equipment Corporation

146 Main Street

Maynard, Massachusetts 01754

CHAPTER 2
INSTALLATION

2.1 SCOPE

This section, in conjunction with the PDP-10 Installation Manual and the Engineering drawings provided in Volume II, contains the information required for MA10/MA10A installation. The following paragraphs contain data which is specific to the memory units but general regarding the remainder of a system.

2.2 UNPACKING

Remove all crating and packing materials, being careful not to damage the equipment. Make a careful visual inspection of the exterior and interior of the equipment. Determine that all modules are correctly seated and repair any mechanical damage. The stack is shipped separately and must be installed according to the instructions contained in Section 5.3.1.

2.3 SITE AND SPACE REQUIREMENTS

There are no special site requirements other than those dictated by environmental conditions (Table 1-1) and service clearances (Figure 2-1). Subflooring is not normally required. The units are free standing and up to four may be bolted together. It is recommended that the memory unit installed closest to the KA10 Central Processor not be separated from it by more than 3 ft* or by less than 1/4 in.

2.4 CABLING

All cables entering or leaving the memory unit cabinets do so through access cutouts under the bottom right and left sides, respectively. Table 2-1 is a cable interconnection diagram.

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*Speedy, the timing program, is written for the standard 10 ft memory bus cable connection between the central processor and the first memory unit. If lengths in excess of 10 ft are used, Speedy timing printouts may not agree with the timing specifications.

2.4.1 Memory Bus

Each memory unit is provided with one set of memory bus cables which is sufficient for operating one of the access ports. The maximum allowable physical length of the memory bus is 100 ft which includes wire runs through each memory unit. For multiport operation, an MC10 option must be obtained for each port which is to be activated. Each MC10 contains one set of memory bus cables which consists of two coaxial cable assemblies terminated in Type W851 Connectors; ten Type W102 Pulse Bus Transceivers are also included. Standard memory bus cable length is 10 ft, unless otherwise specified. The memory bus must be properly terminated in the last memory unit in the system (or in the lone memory unit if only one is installed); proper termination is accomplished through the use of four Type G703 100Ω Terminators in the logic locations indicated for each port in Table 2-1.

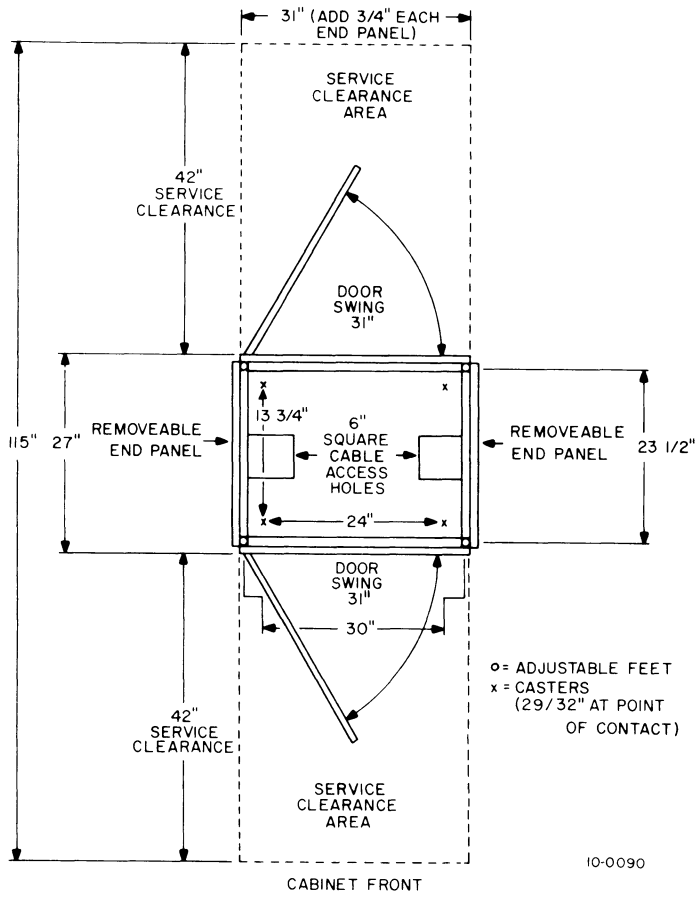

Figure 2-1 MA10/MA10A Core Memory Service Clearances

2.4.2 Power

Each MA10 and MA10A intended for use in the USA is furnished with a 25 ft, 3-wire power cable terminated in a Hubbel #3331 Twist-Lock plug. The #3331 plug mates with the Hubbel #3330 receptacle. Also furnished is a 3-wire ac power cable for remote turn-on and a margin check cable, each cut to the proper length for the particular installation.

2.4.3 Connections

Power is controlled by a Type 844 Power Control mounted on the lower left of the rear plenum door (Figure 1-4). For 115V operation, two orange Faston jumpers must be connected between the pairs of Heyman tabs on the power control. To operate at 230V, the jumpers must be removed.

Table 2-1
Memory Bus Interconnection Chart

MA10 Location	Use	KA10 Location	DF10 Location	MA10 Location	Use	KA10 Location	DF10 Location
ST 19,20	P0 IN CMBI		K, L, 1,2	ST 39,40	P0 IN CMAI		E, F, 1,2
ST 17,18	P0 OUT CMBI			ST 37,38	P0 OUT CMAI		
ST 15,16	P1 IN CMBI	2K, 2L, 1,2		ST 35,36	P1 IN CMAI	2K, 2L, 3,4	
ST 13,14	P1 OUT CMBI			ST 33,34	P1 OUT CMAI		
ST 11,12	P2 IN CMBI			ST 31,32	P2 IN CMAI		
ST 9,10	P2 OUT CMBI			ST 29,30	P2 OUT CMAI		
ST 7,8	P3 IN CMBI			ST 27,28	P3 IN CMAI		
ST 5,6	P3 OUT CMBI			ST 25,26	P3 OUT CMAI		

CHAPTER 3
OPERATION

3.1 SCOPE

This chapter contains information pertinent to the operation of the MA10/MA10A Core Memories. Listings and descriptions of the various controls and indicators and discussions of the address word and the System Block Diagram are included. Figures 3-1, 3-2, and 3-3 illustrate the Power Controls, Switch Panel, and Indicator Panel. Detailed descriptions of operations within the memory units are contained in Chapter 4, Principles of Operation.

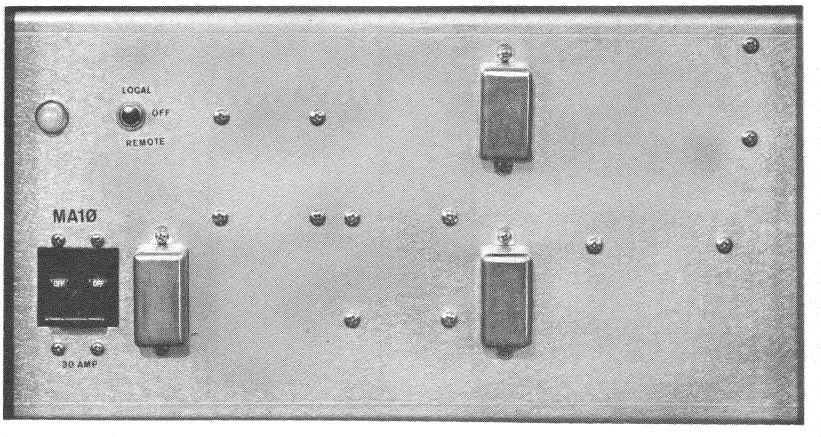

Figure 3-1 Type 844 Power Control Panel

3.2 CONTROLS AND INDICATORS

3.2.1 Power Controls

The MA10/MA10A power controls are situated on the DEC Type 844 Power Control which is mounted on the lower portion of the plenum door. Provided are a 30A ganged toggle-switch type circuit breaker and a LOCAL-OFF-REMOTE toggle switch. The circuit breaker removes all power from the memory unit when in the OFF position. The LOCAL-OFF-REMOTE switch in the REMOTE position allows power to be turned on and off with

the PDP-10 System from the central processor; in the OFF position removes all power from the memory unit power supplies; and, in the LOCAL position applies power to the memory independent of the central processor.

3.2.2 Switch Panel

The control listed in Table 3-1 are mounted on the panel shown in Figure 3-2, which is located at the right side of the logic, and is accessible with the front cabinet door open.

Table 3-1
Controls

Control	Function
SINGLE STEP	When ON, prevents CMC CYC DONE and CMPC AW RQ from being set, thereby allowing one memory cycle to be performed each time the RESTART switch is depressed while a request is asserted.
RESTART	Clears the control and INC.
ERROR STOP	Causes STOP to be set when a control logic error is detected, preventing any further memory cycles until the RESTART switch is depressed.
Pn DES*	Selects or deselects the processor associated with the port. Can also be used to select between the low and high 8K of memory.
NORM/INTL*	Selects normal or interleave operation when more than one 16K (MA10) memory is included in the system.
MADR 18-21*	Select the address of the memory unit.

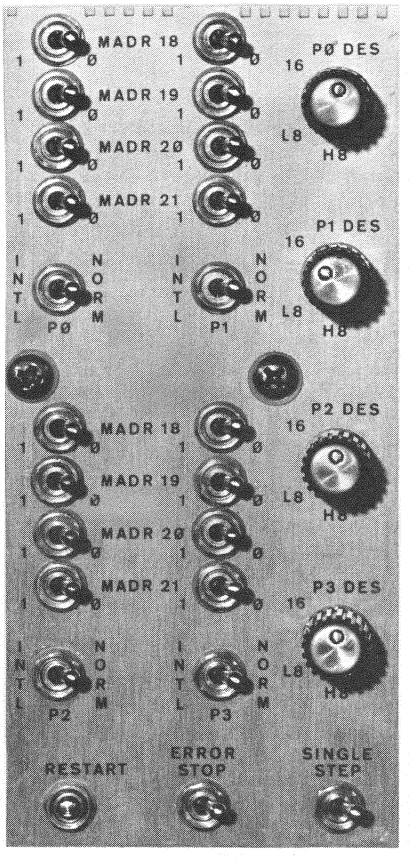

Figure 3-2 Switch Panel

3.2.3 Margin Switches

Margin switches, provided for the performance of margin checks to the logic, are located on the left side of the logic panels and are accessible with the front door open. The logic functions affected by each switch are

*These controls also located on the switch panel are duplicated for each port.

indicated on the switch panels. These switches do not simply control the logic contained in adjacent panels; the wiring is such that each switch applies the margin potential to specific logic functions. The margin switches are illustrated in Figure 3-4.

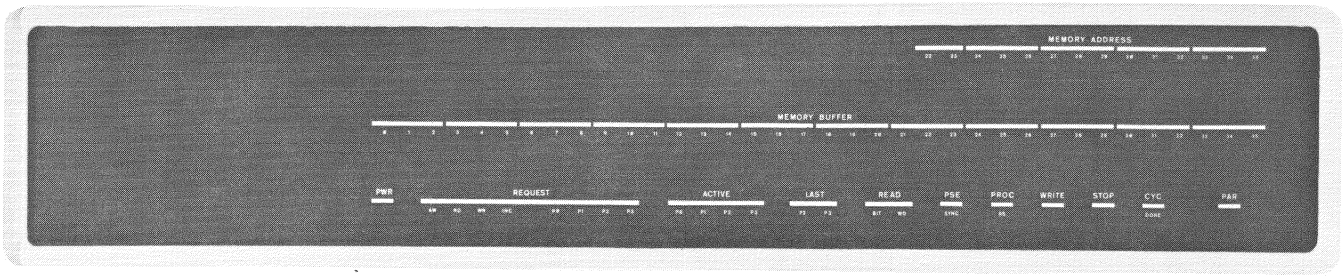

Figure 3-3 Indicator Panel

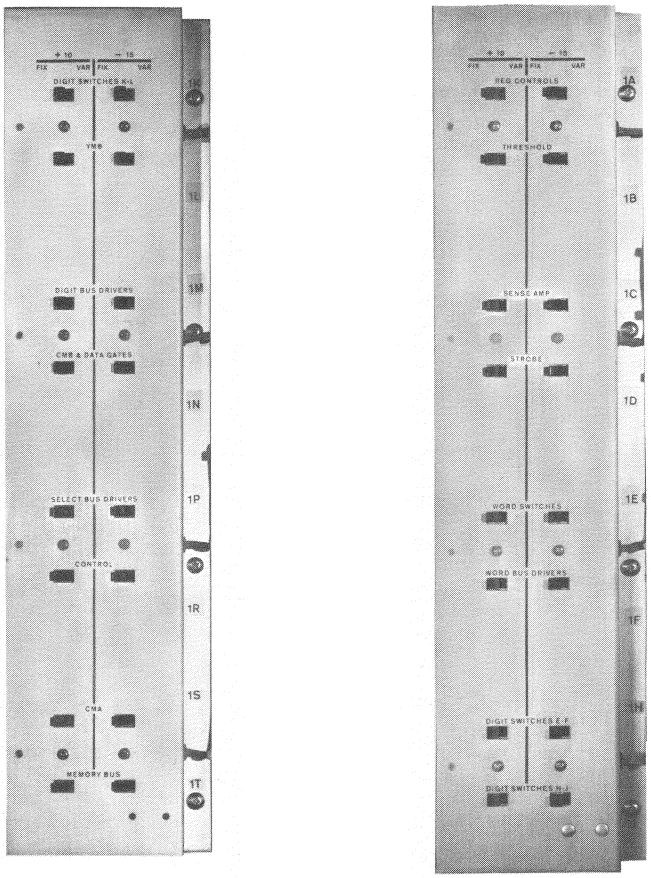

Figure 3-4 Margin Switches

3.2.4 Indicator Lamps

Table 3-2 lists the lamps which are located on the indicator panel.

Table 3-2
Indicator Lamps

Indicator	Meaning
MEMORY ADDRESS (22-35)	Indicates the contents of the CMA buffer.
MEMORY BUFFER (0-35)	Indicates the contents of the CMB buffer.
PWR	Indicates that the memory is energized.
REQUEST	
AW	Indicates that the memory is awaiting a processor request.
RD	Indicates that a read request cycle is being processed or was the last request cycle to be processed.
WR	Indicates that a write request cycle is being processed or was the last request cycle to be processed.
RD and WR	Indicates that a read-modify-write request cycle is being processed or was the last request cycle to be processed.
INC	Indicates that an illegitimate processor request has occurred. (Remains on until the RESTART button is depressed or until power is reapplied.)
P0	Processor 0 memory cycle request.
P1	Processor 1 memory cycle request.
P2	Processor 2 memory cycle request.
P3	Processor 3 memory cycle request.
ACTIVE	
P0	Processor 0 has gained access.
P1	Processor 1 has gained access.
P2	Processor 2 has gained access.
P3	Processor 3 has gained access.
LAST	
P2	Of processors P2 and P3, P2 has last gained access.
P3	Of processors P2 and P3, P3 has last gained access.
READ	
BIT	Indicates that bit read current is on.
WR	Indicates that word read current is on.

Table 3-2 (Cont)
Indicator Lamps

Indicator	Meaning
PSE SYNC	Indicates the end of the read portion of a memory cycle.
PROC RS	Indicates the performance of a clear-write cycle or read-modify-write cycle.
WRITE	Indicates that both bit and word write currents are on.
STOP	Indicates single step operation or the detection of a control logic error while in the error stop mode.
CYC DONE	Indicates the completion of a memory cycle.
PAR	Indicates the state of the CMC PARITY flip-flop.

3.3 OPERATIONAL DESCRIPTION

The memory address word transmitted to the CMPC over the MADR lines has the following form:

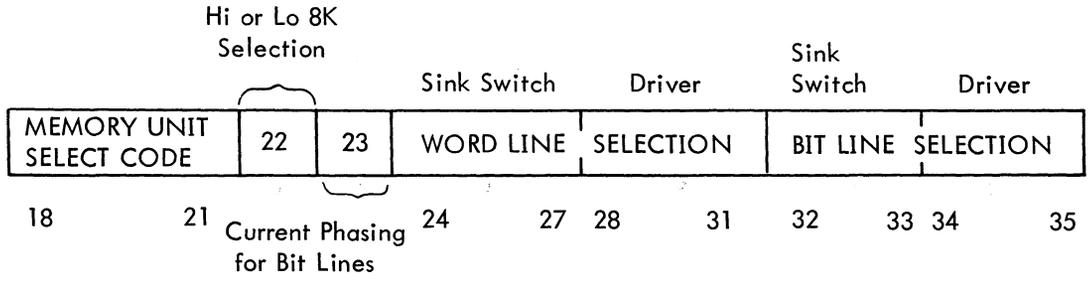

Figure 3-5 Memory Address Word

Figure 3-6 is the System Block Diagram of the MA10 Memory Unit. MADR lines carry the cycle requests and memory address information from the processor to the memory unit. The settings of the MADR (18-21) switches in the core memory processor control determine through which port the memory is accessed. When bits 18-21 of the MADR word match the switch settings of a port in a particular memory unit, the processor connected to that port will gain access to the memory unit if the additional enabling conditions for access are true (Section 4.3). Since each memory unit has four access ports, operation with up to four independent processors is possible. Priority logic contained within the MA10 is provided to establish the sequence of memory unit access

when two or more ports are addressed simultaneously. The processor associated with port 0 has first priority, while that connected to port 1 is assigned second priority. Third and fourth priorities are shared by ports 2 and 3, and priority is assigned to that port (P2 or P3) which did not last have access to the memory unit.

After access has been granted and processor priority has been established, the controls necessary for data storage or retrieval are generated. Read and write control is transmitted to the memory unit from the processor over the MADR lines by means of WR RQ and RD RQ signals which occur simultaneously with the memory address word. If both WR RQ and RD RQ are asserted, the operation is a read-modify-write cycle.

As shown in Figure 3-5, bit 22 of the MADR word (CMA22) determines which pair of planes in the stack, high or low 8K segment, will be read from or written into. Figure 4-5 illustrates the stack configuration. Bit 23 controls the current phasing for bit lines; e.g., specifies the direction of digit current, and is therefore used to cause word and bit current to add in one plane and cancel in another. Bits 22 and 23 together select one of the four planes: 22(0), 23(0) - Plane 0; 22(0), 23(1) - Plane 1; 22(1), 23(0) - Plane 2; 22(1), 23(1) - Plane 3. MADR bits 24 through 31 form the word selection matrices and bits 32 through 35 form the digit selection matrices. Word selection matrices consist of 256 lines for low 8K and 256 lines for high 8K. Digit selection matrices consist of 37 redundant 16 line matrices for a total of 592 bit lines. Each bit of a 37-bit word is composed of 256 word selection lines and 16 digit selection lines per plane which allows memory word storage in one of 4096 locations, on one of four planes. One memory location is determined from the selection of one word line and one digit line for 37-bits of the address.

During read, both digit and word currents in the stack are turned on. The data outputs from the selected location are placed on the MBD lines through the sense amplifiers. Upon completion of the read operation, all memory cores of the addressed location are in the 0 state.

When writing, word current is always turned on, however, digit current is controlled by the data word and is turned on only when a 1 is written. When a 1 is to be stored in a bit location, one digit line and one word line will be selected. When a 0 is to be stored in a bit location, none of the digit lines for that location is selected.

3.3.1 Interleaving

The logic allows pairs of 16K memory units to be arranged in such a manner that consecutive addresses alternate between the memory units in the pair. The MADR bit-21 selector switch at the first memory unit (n) must be on a 0 and the corresponding switch at the second memory unit (n + 1) must be on a 1. Memory unit requirements for interleaving are that only adjacent units designated n and n + 1, where n is even, may constitute the interleaving pair. Pairs composed of 0 and 1 or 2 and 3 or 4 and 5 are proper arrangements while 1 and 2 or 0 and 2 are improper interleaving pairs.

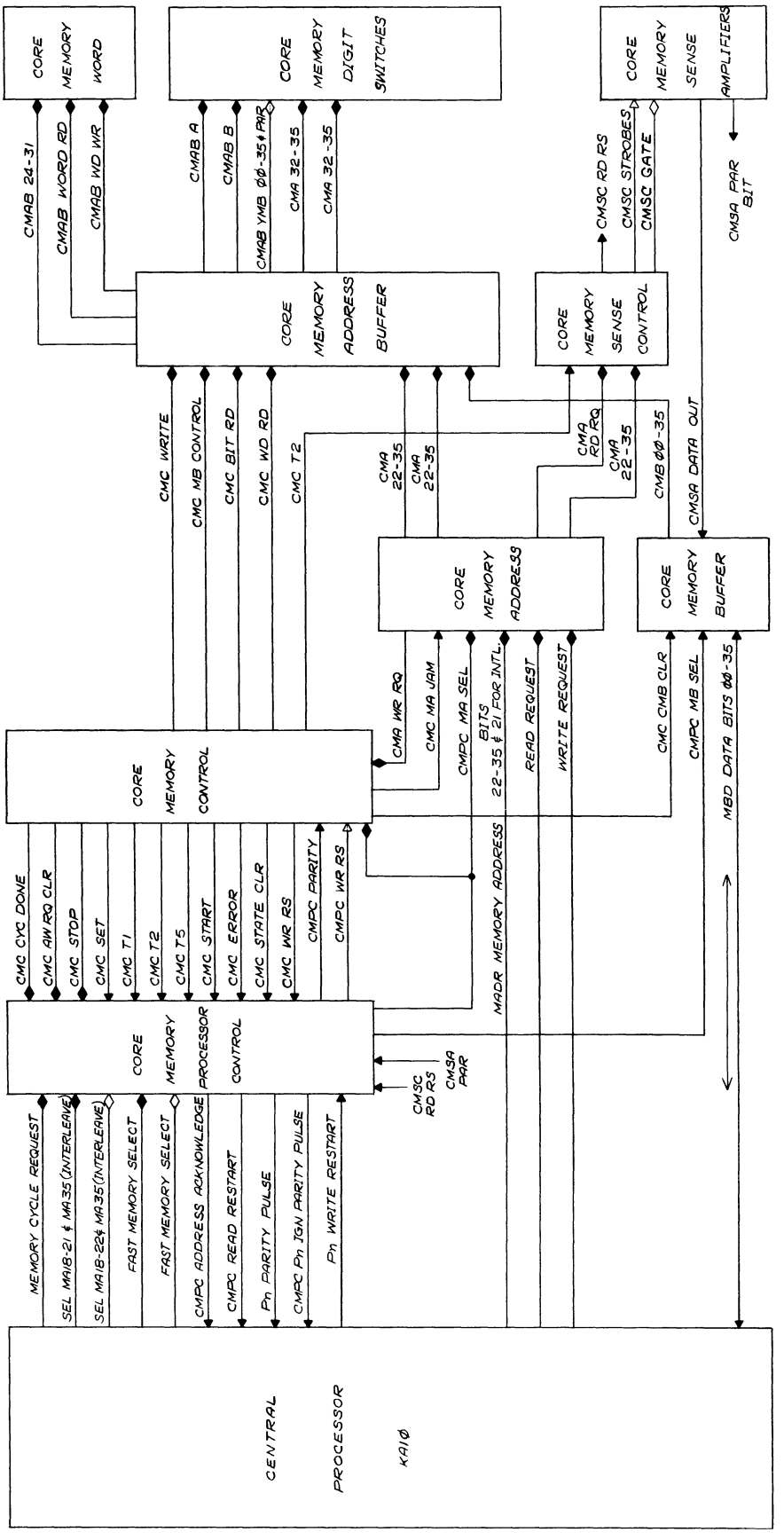

Figure 3-6 System Block Diagram

The interleave mode is entered by manually setting the INTL/NORM switch on the switch panel at each memory unit of the pair to the INTL position. An examination of the form of the MADR word (Section 3.3) reveals that in the interleave mode, the least significant bit of the bit line selection bits (bit 35) is interchanged with the least significant bit of the memory unit selection bits (bit 21). MADR words ending in 0s (bit 35) will therefore cause selection of the memory unit designated n while words ending in 1s will cause the unit designated n + 1 to be selected. As bit 35 now represents the most significant bit of the address word, all addresses in memory unit n are even locations and all addresses in memory unit n + 1 are odd.

CHAPTER 4
PRINCIPLES OF OPERATION

4.1 SCOPE

Each section of the logic is discussed in the following paragraphs. Flow charts relevant to each section are interspaced throughout the chapter. Reference is made only to these charts and to the engineering drawings contained in Volume II. Appendix A is an alphabetical list of mnemonics. Appendix B contains a tabulation of logic peculiar to MA10 Serial Nos. 3-59. Appendix C is a discussion of core memory fundamentals which supplements the Stack Organization discussion, Section 4.6.

4.2 INITIAL CONDITIONS

Figure 4-1 is a flow chart showing the sequence of operations which occur within the MA10 from the time power is applied until the memory is ready to accept a request for access from a processor. Also illustrated are those operations which take place during power interrupt and logic error conditions.

The ~PSOK level is asserted when improper power supply operation or power interrupt conditions exist. This level, developed from the G816 Regulator Control in the CMPR, generates the CMC AW RQ CLR level which clears CMPC AW RQ. If ~PSOK remains asserted for 100 μs, CMC PWR CLR (0) is generated clearing CMC BIT RD, WORD RD, and WRITE. This turns off all read and write current to the stack through three OR gates. ~PSOK, therefore, effectively stops the memory unit operation after completion of the cycle in progress. The memory unit will remain in this state until PSOK is asserted. No manual restart is necessary under these conditions.

Assertion of PSOK, indicating normal power supply potentials, after a 200 ms delay, causes generation of CMC PWR START. This pulse or CMC RESTART (obtained from manually operating the RESTART pushbutton) causes the generation of CMC START, CMC RESET, and, after a 116 ns delay, CMC SET. CMC START collector-clears the CMPC INC RQ and CMC STOP flip-flops. CMC RESET causes generation of CMC STATE CLR and resets the CMC MB CONTROL flip-flop. CMC SET, as CMC STOP is cleared, sets the CMC CYC DONE and CMPC AW RQ flip-flops. The performance of these operations places the memory unit in an idle state ready to respond to access requests.

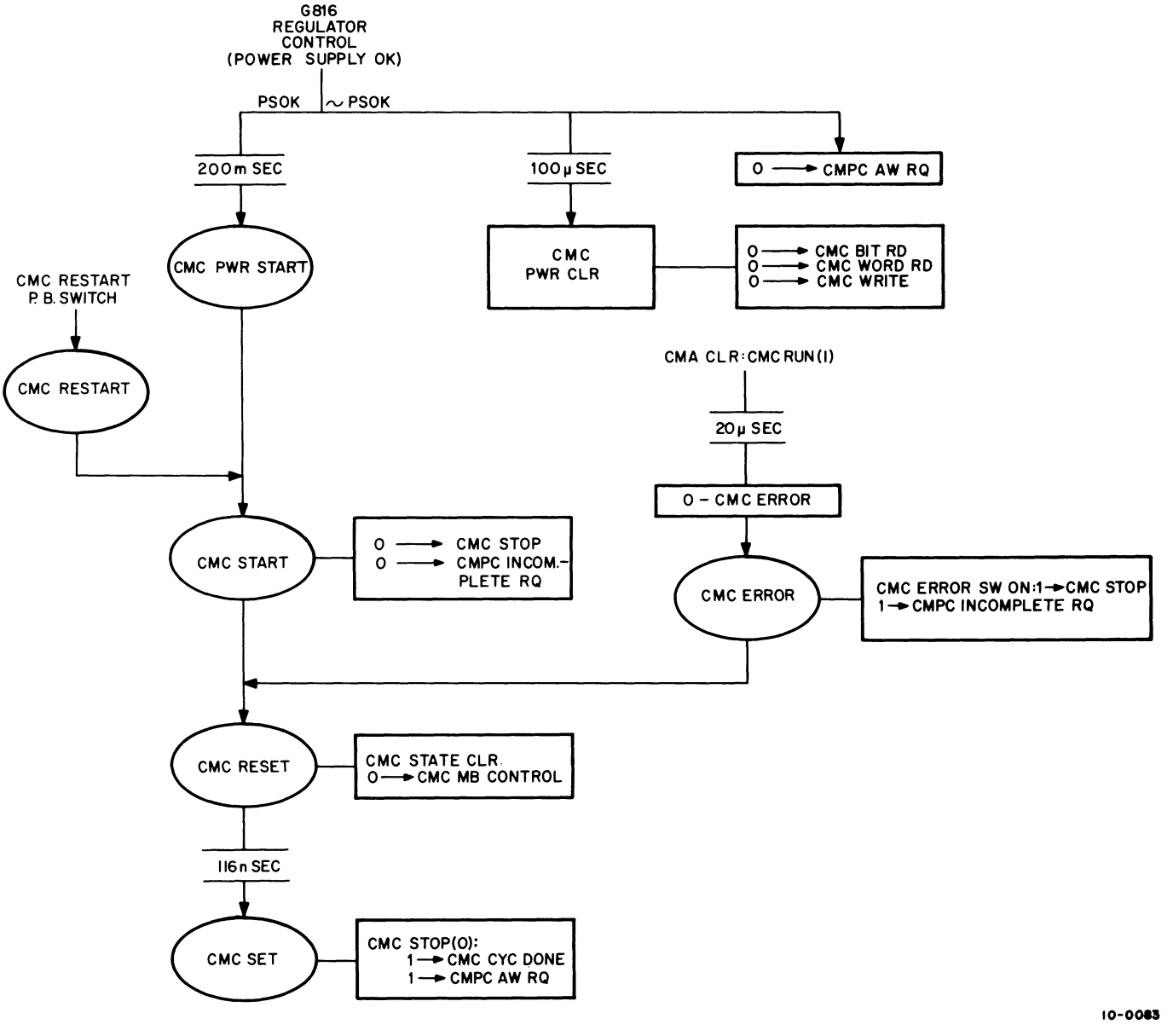

Figure 4-1 Initial Condition Flow Chart

If, for any reason, CMC RUN remains in the set condition for 20 μs or more (far in excess of the time required for any memory cycle), CMC ERROR is generated setting CMC INC RQ and lighting the INC RQ lamp on the indicator panel. This condition, with the CMC ERROR STOP switch in the ON position, collector-sets the CMC STOP flip-flop. CMC STOP (1) prevents the setting of CMC CYC DONE and CMPC AW RQ. In this situation the memory unit is hung-up and must be manually restarted by CMC RESTART, generated by depressing the RESTART switch.

4.3 REQUEST LOGIC

Upon termination of the initializing period, the CMC CYC DONE and CMPC AW RQ flip-flops are set and the memory unit is in the idle condition. This section describes the operations which take place within the memory unit upon receipt of an access request from a processor. The discussion refers to Figure 4-2, the Request-Acknowledge Flow Chart.

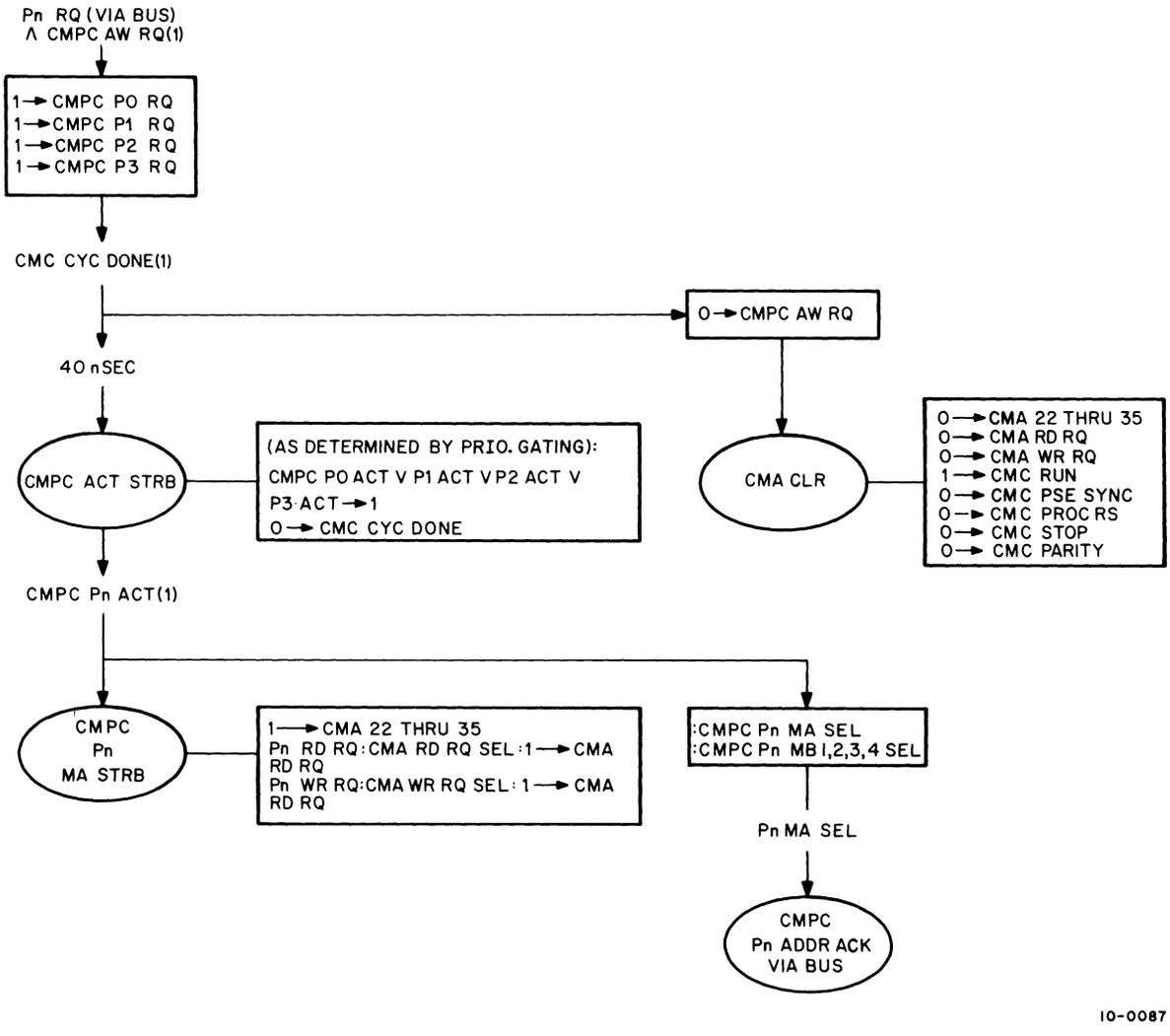

Figure 4-2 Request-Acknowledge Flow Chart

Contained in the CMPC logic are four flip-flops designated CMPC P0-P3 RQ, each of which is associated with one of the four memory unit access ports. Setting of a CMPC Pn RQ flip-flop depends upon the enabling of a 12-input NAND gate. Referring to sheet 1 of the CMPC drawing, it can be seen that each NAND gate contains a CMPC AW RQ (1) input at pin M. This level is the output of the CMPC AW RQ flip-flop set at CMC

SET time of the initialize phase. The next four inputs (to pins N, P, R, and S) select MADR bits 18(0) or (1) through 21(0) or (1). This is the memory unit selection network. When the switch settings match the configuration of MADR bits 18 through 21 of the address word, all four inputs for one gate will be true. As each gate has its own set of switches, each port may be set to respond to different address codes from the processors associated with the individual ports. Pin S has an additional qualification in that it is connected through another switching network which allows substitution of MADR bit 35 for MADR bit 21 and bit 21 for 35. This is the INTERLEAVE switch. With a pair of memories designated n and n + 1 and with the INTL switch ON, the port selection will depend on bit 35 of the address word. When bit 35 (0), the memory unit designated n will be selected; when bit 35(1), n + 1 will be selected. ~FMC SELECT is a level provided from the PDP-10 processor for operation in systems with memory units containing accumulator sections. This level will always be held at -3V for input to MA10/MA10A Memory Units when in PDP-10 configurations. This level is used by the PDP-6 with fast AC units. The input to pin U is the REQUEST CYC signal from the processor. The remaining input to pin V is asserted through 4-position wafer switches. In the first position, DES, a ground is applied to pin V disabling the gate; this deselects the processor associated with that port from the memory. The second position, 16, applies -3V to pin V which enables the gate if the remaining inputs are true. Positions L8 and H8 of the switch are provided for operation with MA10A (8K) systems where the addressing of locations 0-8K is designated by MADR bit 22 of that memory unit on a 0 and the addressing of locations 8K-16K (in another MA10A) is designated by MADR bit 22 on a 1.

When all the inputs to either or all of the selection gates are true, the gate(s) is/are enabled resulting in the collector setting of the associated CMPC Pn RQ flip-flop(s).

CMC CYC DONE(1), which is set by the CMC SET pulse and CMC STOP(0) during the initialize phase, and CMPC Pn RQ(1) generate CMPC AW RQ(0). The positive-going transition of this level generates CMA CLR through a pulse amplifier. CMA CLR performs the following functions:

a. Direct clears the CMA Register
b. Clears CMC PSE SYNC, CMC PROC RS, CMC STOP, and CMC PARITY
c. Clears CMA RD RQ and CMA WR RQ
d. Sets CMC RUN

The CMPC AW RQ(0) condition precludes acceptance of processor access requests (this flip-flop is set 141 ns after CMC T5 time, which is approximately 500 ns into the memory cycle). Clearing the several control flip-flops and setting CMC RUN readies the memory unit for performing the type of request the processor has made, i.e., read, write, read-modify-write.

At this point, one or more of the CMPC Pn RQ flip-flops are set and the CMPC logic assigns priorities to each access port to allow only one processor access at one time.

The outputs of the CMPC Pn RQ flip-flops are applied to an OR gate where any RQ level on a 1 and DONE(1) cause generation of CMPC ACT STRB after a 40 ns delay. This level is applied to each of six NAND gates at the input to the priority selection logic.

Enabling of each gate is inhibited if a CMPC Pn RQ(1) is asserted which is of lower designation than the CMPC Pn ACT flip-flop with which the gate is associated. First priority is therefore assigned to P0, and second priority to P1. Third and fourth priorities are shared between P2 and P3 in the following manner. CMPC P3 LAST and CMPC P2 LAST are developed in a flip-flop which is set and cleared by the P3 and P2 ACT flip-flops, respectively. This flip-flop remembers which of P2 or P3 last gained access. Its output applied to the P2 and P3 gating, in the event of simultaneous requests, inhibits access for the processor which has last been serviced.

The assertion of CMPC ACT STRB and CMPC Pn RQ(1) have, therefore, enabled one of the six gates, depending upon which processor has requested access. If CMPC P0 RQ(1) is asserted, CMPC P0 ACT is collector-set and the processor associated with port 0 gains access to the memory unit. The following levels are generated in the CMPC logic as a result of setting CMPC P0 ACT: CMPC P0 MB SEL 1-4, CMPC P0 MA SEL, and CMPC P0 MA STRB.

In the CMA logic, the assertion of CMPC P0 MA STRB causes the 1s contained in MADR bits 22 through 35 to be read into the CMA Register. The condition of CMA 35 depends upon the mode of operation: if interleaving, bit 21 is read-in; if normal, CMA 35 is loaded from MADR bit 35. The remaining two flip-flops in the CMA determine the type of request being made by the processor and are also set by signals from the processor over the MADR lines. If this is to be a read cycle, only CMA RD RQ is set; if a clear-write cycle is requested, CMA WR RQ is set; while if a read-modify-write cycle is requested, both flip-flops are set.

CMPC P0 MA SEL generates CMPC P0 ADDR ACK over an MADR line to the processor. This pulse serves to advise the processor that the address contained in the MADR word has been brought into the CMA and that the memory unit has begun its cycle.

CMPC P0 MB SEL 1-4 enable the gating in the CMB logic which allows the sense amplifiers to place the data stored in the addressed location in the CMB. The contents of CMSA00-23 are ANDed with CMPC P0 MB SEL 3 and CMPC P0 MB SEL 1 to collector-set the corresponding CMB flip-flop (CMB00-23) for each 1 sensed by the sense amplifiers. Enabling of the gates for the loading of CMB24-35 is dependent upon the 1s contained in CMSA24-35 and upon the assertion of CMPC P0 MB SEL 4 and CMPC P0 MB SEL 2. This gating is duplicated for each of the remaining three ports (P1, P2, and P3).

4.4 READ LOGIC

This section describes the events which occur in the memory unit subsequent to assertion of the ADDR ACK pulse. Figure 4-3 is the READ Flow Chart. Descriptions of word and digit line selection are contained in Section 4.6. Appendix C contains a general discussion of core memories.

Upon completion of the request-acknowledge phase, CMA is loaded with the 1s contained in bits 22 through 35 of the MADR word. These are the bits which determine the location within the stack which will be read from. The processor issues a Pn RD RQ simultaneously with the address word which, ANDed with CMPC Pn MA STRB, causes generation of CMA RD RQ and results in generation of the CMA RD RQ SEL level by the same gate which sets CMA RD RQ. CMA RD RQ or CMA WR RQ SEL generates CMC T1. CMC T2 through T4 are derived from CMC T1 and possess delays of 80 ns*, 216 ns, and 70 ns, respectively.

CMC T1 collector-sets CMC BIT RD which turns on the bit read current in the stack. CMC T1 also causes CMC CMB CLR 1 and CMC CMB CLR 2 to be generated; these pulses clear the CMB. The assertion of CMC T2, 80 ns* later, sets CMC WORD RD causing word current to be turned on in the stack. At this point, both bit and word currents are turned on and the CMB is cleared. CMC T2 also sets or clears CMPC LAST PROC at this time, if either CMPC P2 ACT or CMPC P3 ACT is set. These levels are asserted at the priority selection gates as described in Section 4.3.

The delay between the turning on of bit and word read currents (the time between the generation of T1 and T2) is "stagger time". Depending upon the type of stack installed, this delay is either 60 ns or 80 ns and is derived from the Type B312 Adjustable Delay Line in logic location N40. Stagger time is provided to allow noise caused by the turning on of bit current to decay to a value which cannot be construed as a 1 output by the sense circuitry.

As this is a read cycle, (CMA RD RQ(1)), CMSC STROBE, CMSC STROBE RS, and CMSC RD RS are generated. CMSC STROBE initiates generation of CMSC STROBE (0-8), (9-17), (18-26) and (27-par). The data sensed is loaded into the CMB from the sense amplifiers. CMSC RD RS is transmitted to the processor on an MADR line and serves to advise the processor that there is a data word on the memory bus. The addressed location's content has been set to 0 during the read operation.

CMC T3 causes CMC BIT RD and CMC WORD RD to be reset, turning off both bit and word currents in the stack. CMC T4 which is generated 70 ns after CMC T3 sets CMC PSE SYNC, if either CMA RD RQ or CMA WR RQ are on 1s. If this is a clear-write cycle, the events are the same except that CMSC STROBE is not generated and the contents of the location are not read into CMB. If, however, this is a read-modify-write cycle, CMSC

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*Delay is dependent upon type of stack installed. Refer to drawing D-BS-MA10-0-CMC-B for specific information.

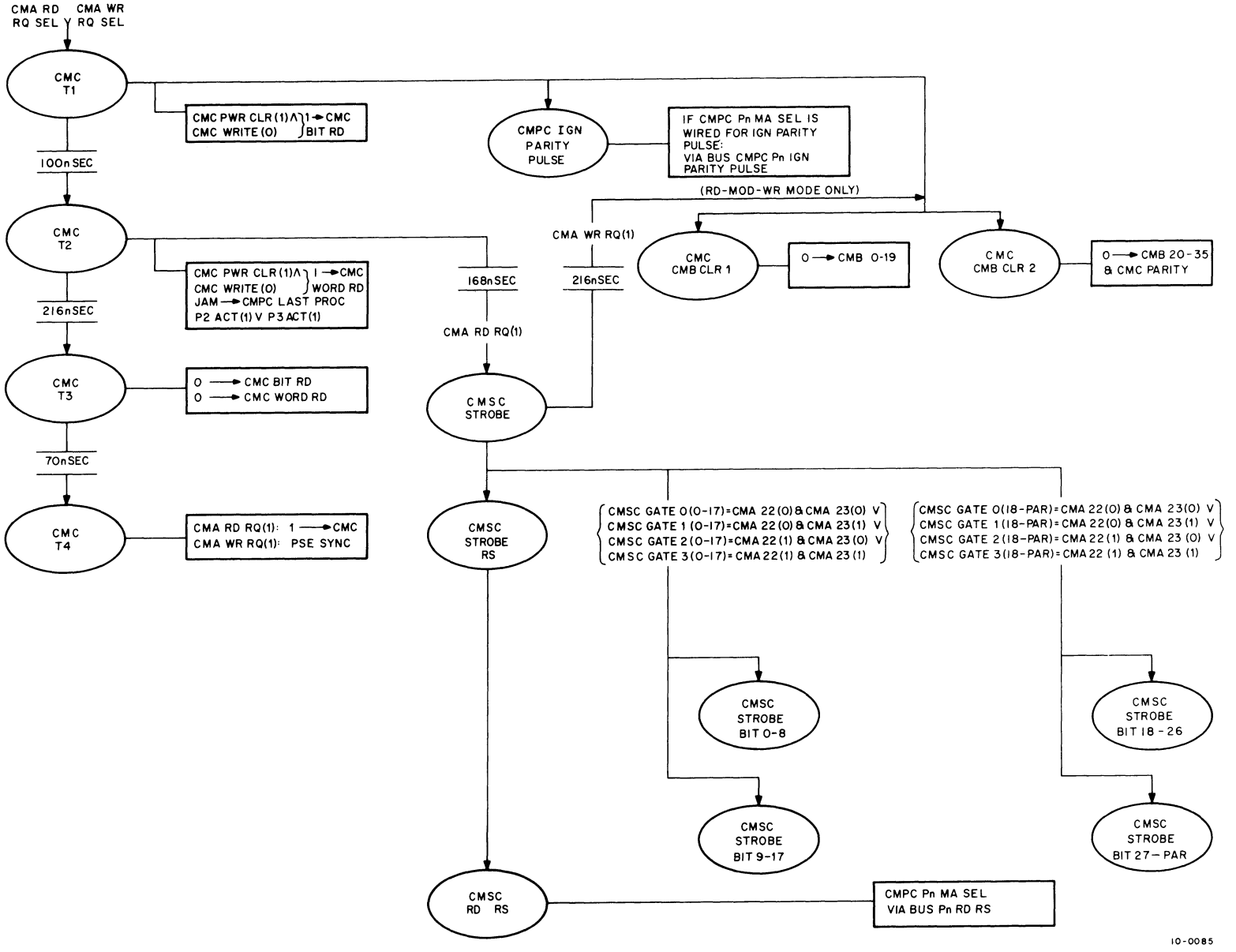


Figure 4-3 Read Flow Chart

STROBE is generated, the data is read into the CMB, and after a delay of 216 ns the generation of CMC CMB CLR 1 and CMC CMB CLR 2, as at CMC T1, clears CMB.

At this point, therefore, regardless of the type of cycle in progress, the location contains 0s. If this is a read operation, the data is in the CMB and is written into the same location; if a write operation, the processor brings up WR RS and places data on the memory bus to be written into the location; and if a read-modify-write operation, the memory remains connected to the processor while the processor performs some operation on the data read from memory and then brings up WR RS and places the modified word on the memory bus.

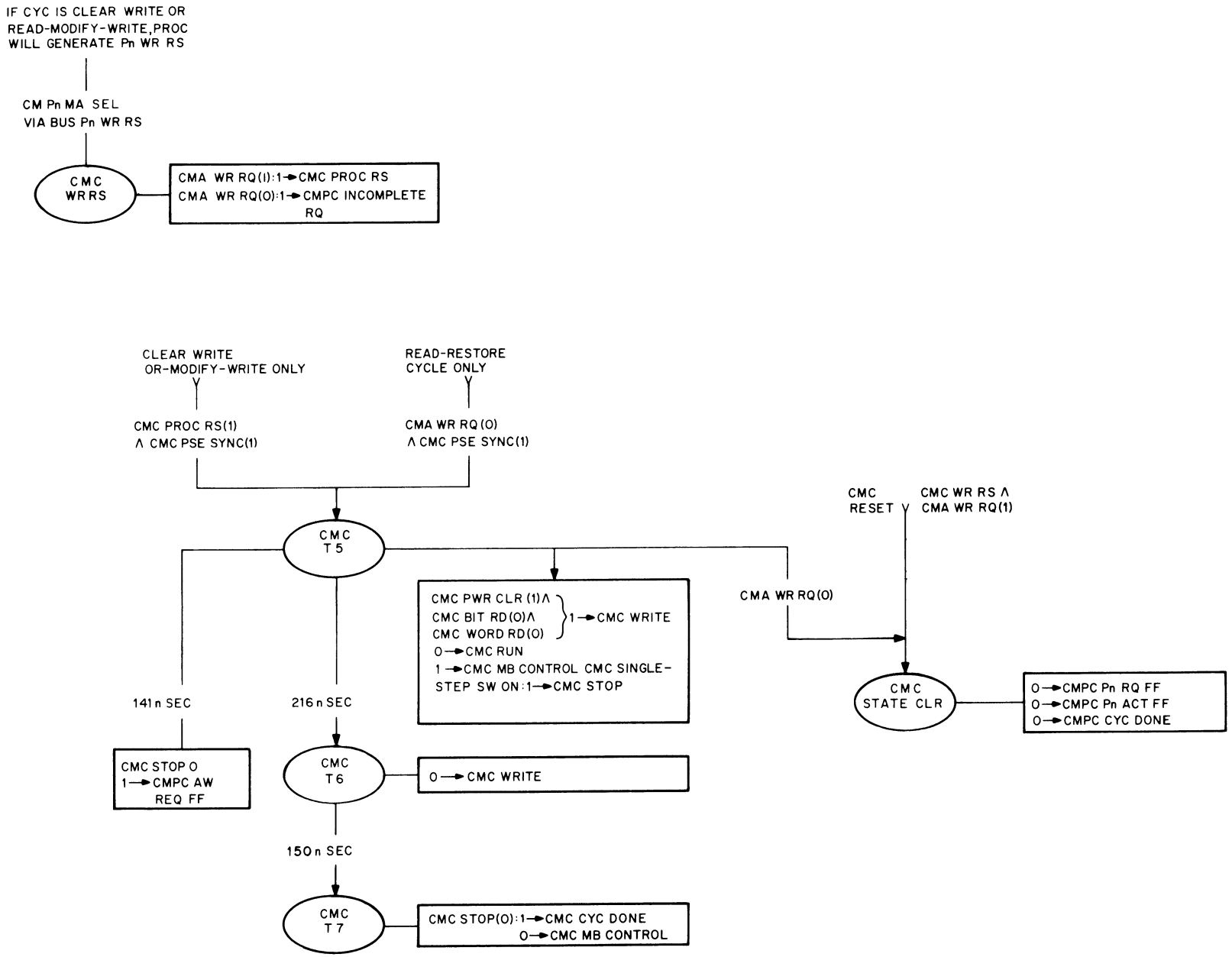
4.5 WRITE LOGIC

This section describes the events which take place within the memory unit during the write portion of the memory cycle, either while the restore portion of a READ operation is in progress or while the memory unit is performing a clear-write or read-modify-write operation. The flow-chart to which this discussion refers is Figure 4-4.

If this is a read-restore operation, bit and word currents to the stack are turned off after strobing at time T3 and CMC PSE SYNC is set at time T4. If CMA WR RQ (0) and CMC PSE SYNC (1) and CMC CYC DONE (0) are asserted, timing pulse CMC T5 is generated triggering T6 and T7 after fixed delays. CMC T5 collector-sets CMC WRITE, CMC MB CONTROL and clears CMC RUN. CMC WRITE turns on the bit and word currents in the stack initiating the writing-in of the data contained in the CMB and restoring to the addressed location the data which was placed on the memory bus for the processor's use during the read operation. CMC WRITE (1) also clears CMC BIT RD and CMC WORD RD. CMC MB CONTROL (1) generates CMAB MB CONTROL 1-6 in the CMAB logic. These levels control the writing of data. Writing of a 0 is accomplished by disabling the CMAB YMB level. If the SINGLE STEP switch is ON, CMC STOP is set at CMC T5 time, also. With CMC STOP (0), CMPC AW RQ is set 141 ns after assertion of T5. This condition allows a processor to gain access to the memory unit even though the current memory cycle has not been completed. The CMPC Pn ACT flip-flop, however, is not set until CMC CYC DONE is set at CMC T7.

Assertion of CMC T6, clears the CMC WRITE flip-flop which turns off stack bit and word line currents. If CMC STOP is cleared, the final timing pulse, CMC T7, sets CMC CYC DONE which in turn sets a CMPC Pn ACT flip-flop, if a processor request has been asserted, and clears CMC MB CONTROL.

If this is a write or read-modify-write cycle, the processor responds with data on the memory bus simultaneously with a Pn WR RS pulse over an MADR line which results in the generation of CMPC WR RS. This pulse generates CMC WR RS and CMC PROC RS, if CMA WR RQ (1) is asserted. If CMA WR RQ (1) is not asserted, the CMPC INC RQ flip-flop is set. CMC PSE SYNC was set at CMC T4 and this condition ANDed with CMC PROC RS allows generation of CMC T5, as before. The remaining operations are identical with those described in connection with the restore portion of the read-restore cycle.



10-0086

Figure 4-4 Write Flow Chart

4.6 STACK ORGANIZATION

Figure 4-5 illustrates the planar construction of the MA10 stack. It is composed of four interconnected planes, where each plane consists of thirty-six 64 x 64 core arrays and four 64 x 16 core arrays arranged in a matrix (also shown in Figure 4-5). Each 64 x 64 core array is logically subdivided into four 16-core channels where each channel represents one bit per word in the bit or digit dimension. The MA10A stack is composed of two interconnected planes; the interconnections and remainder of the stack configuration are identical to those of the MA10. Figure 4-7 is the Magnetics Logic Block Diagram.

There are 256 (64 x 4) word lines in the word dimension for each plane. As shown in Figure 4-5, the top two planes are interconnected in such a manner that each word line threads 1184 [(64 x 9) + 16] [2] cores. The remaining two planes are connected in a similar manner. There are, therefore, two word line segments each containing 256 lines.

Each sense line will sense 256 (64 x 4) cores in the word dimension and 16 cores in the digit dimension for each plane. This allows each sense line to sense 4096 cores per plane. There are four sense lines for each digit, one on each plane, for a total of 148 (37 x 4). The sense line windings are of a "bow tie" configuration as shown in Figure 4-9. Crossovers occur between core pairs in the digit dimension and every 64 cores in the word dimension.

There are 16 digit lines for each 16K word bit. One of 16 digit lines is selected by means of a 4 x 4 two-diode-per-line decoding matrix as shown in Figure 4-6. The diode end of the line is referred to as the drive point and the other end as the sink point. There are eight drive points and four sink points for each bit. For all 37 bits, there are 296 drive points and 148 sink points hand-wired to 37 Type W014 Interconnection Boards. Four consecutive digit lines are bussed together to form one sink point, while a drive point is formed by tying every fourth diode point together.

Selection of a word line for each 256 word line segment is accomplished by a 16 x 16 two-diode-per-line matrix, as shown in Figure 4-6. There are, therefore, 512 diodes per segment or 1024 diodes per 16K stack. Each 256 word line segment has 32 drive points and 16 sink points. The sink and drive points are hand-wired to W013 and W017 Interconnection Boards, respectively. Every sixteenth sink end is bussed together to form a sink point. Sixteen consecutive diode anodes are bussed together to form a read drive point and sixteen consecutive diode cathodes are bussed together to form a write drive point.

The four sense windings of each digit are hand-wired to a 9-pin Cannon male connector. All 37 connectors are mounted on a bracket attached to the top rear of the stack as shown in Figure 4-8. The extra pin in each connector is provided for connection to stack ground. One stack ground is brought out for each six bits. The winding order is such that the word drive line is placed between the sense winding and the digit drive line.

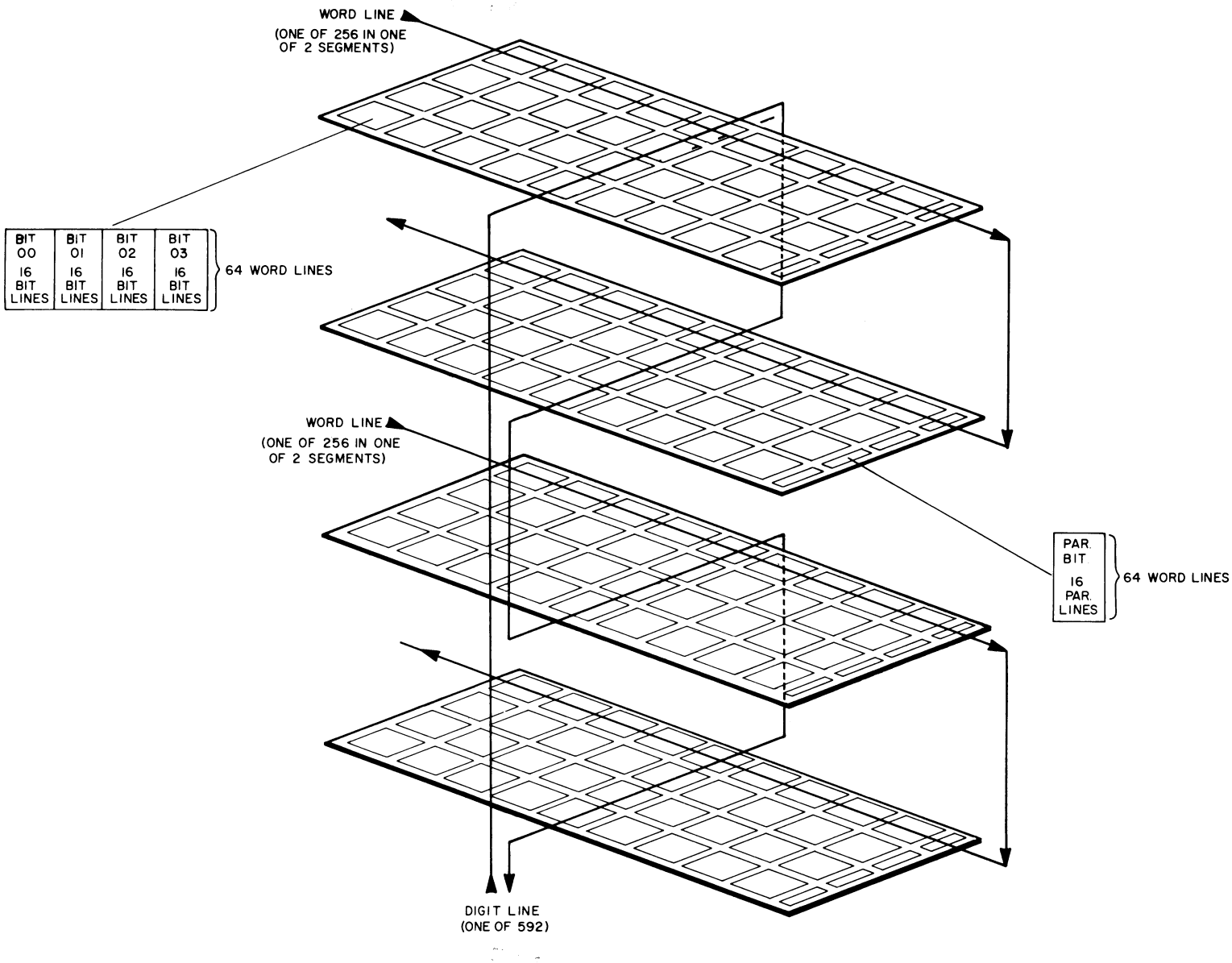


Figure 4-5 Stack Organization

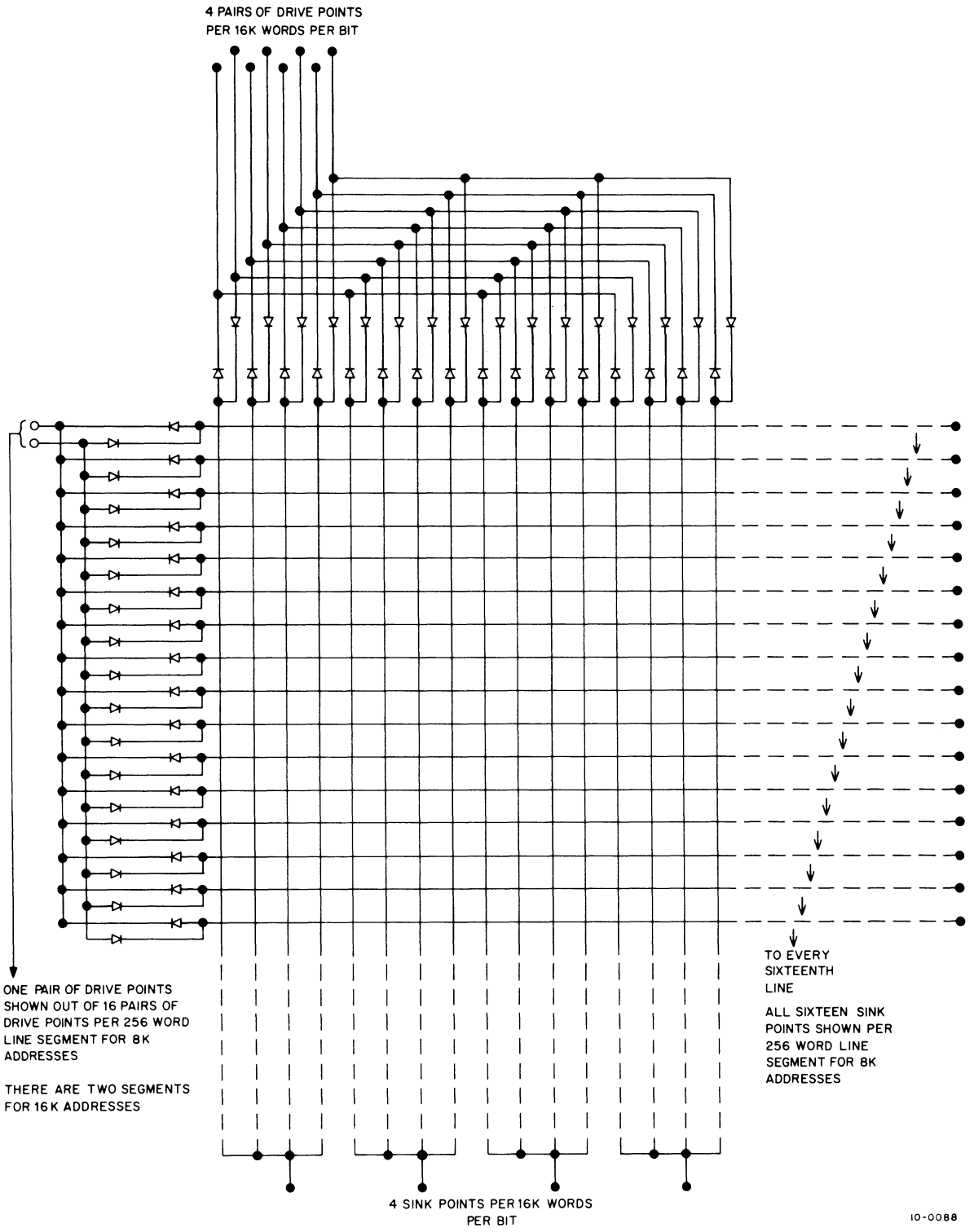


Figure 4-6 Decoding Matrices

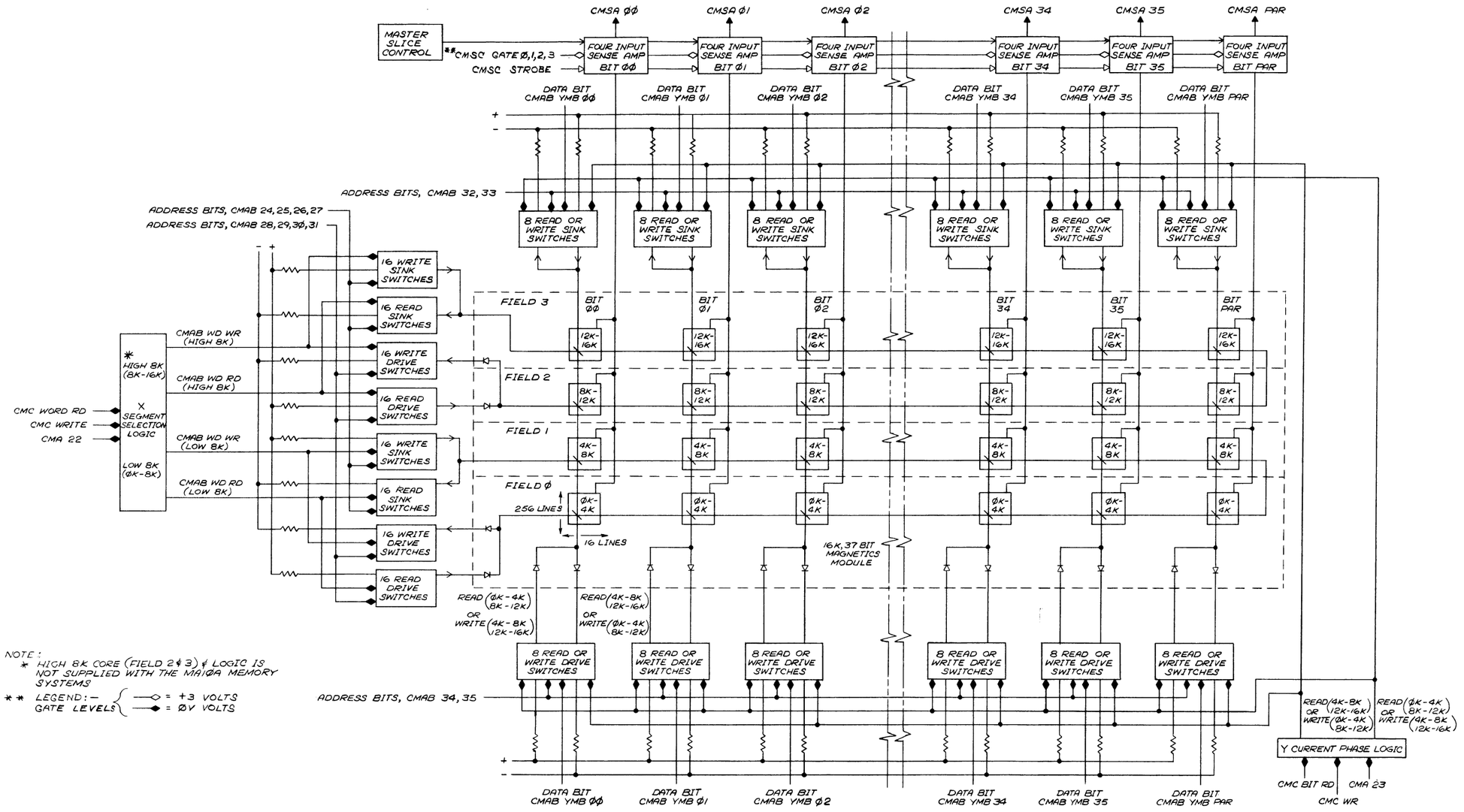


Figure 4-7 Magnetics Logic Block Diagram

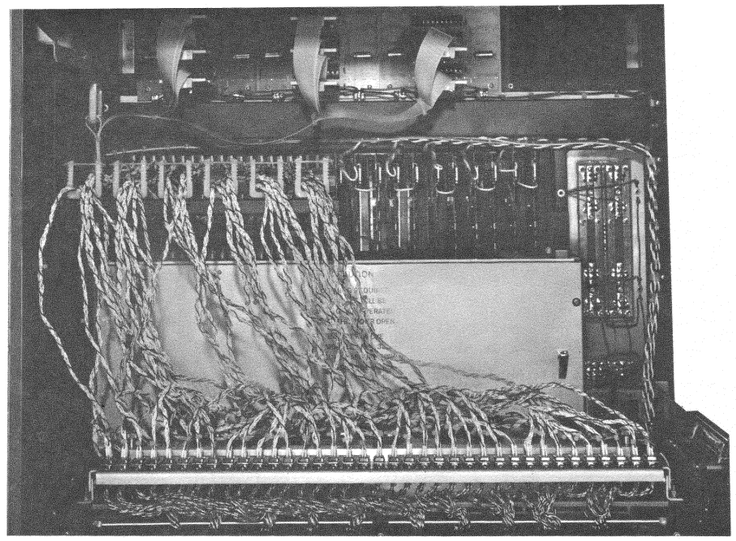


Figure 4-8 Stack Connectors

4.6.1 Digit Line Selection

Two Type G219 Memory Selectors control selection among the 16 digit lines for each bit. Only one of the eight current switches contained in each G219 module is turned on at any one time. Phasing of the drive currents is performed in the digit dimension; the direction of digit read current into the lines is opposite for alternate planes and is controlled by bit 23 of the MADR word. Read current enters the stack through the diode end and exits through the sink end for the first 4096 and third 4096 words. The opposite is true for the second and fourth planes. For example, from sheet 1 of the CMDS drawing, CMAB B (00-05) 1 and CMAB B (00-05) 2 will be asserted to turn on the read current in 1 of the 16 lines in bit 0 for a core located on the first or third plane. For writing, CMAB A (00-05) 1 and CMAB A (00-05) 2 will be asserted for the first or third plane and CMAB B (00-05) 1 and CMAB (00-05) 2 will be asserted for the second or fourth plane.

MADR bits 32, 33, 34, and 35 are used to select one of the 16 digit lines. The buffering of these lines is shown on the CMAB drawing which also illustrates the logic which generates the ~ CMAB YMB levels. Writing of a 0 is accomplished by disabling the CMAB YMB level associated with the addressed bit during the writing portion of the cycle. This condition occurs with CMAB MB control (1) and the corresponding CMB bit on a 0. The data word therefore controls the writing of data in the digit dimension. One ~ CMAB YMB level is generated for each 0 contained in the CMB.

4.6.2 Word Line Selection

Eight Type G217 Memory Selector modules are used for selection among the 256 word lines for each 8192 word segment. Selection of one of the two segments is accomplished by the CMAB WD RD 1, 2 and CMAB WD WR 1, 2 levels. These levels are conditioned by the state of bit 22 of the MADR word. The direction of the read current is always into the drive end and out the sink end while the write current is in the opposite direction.

4.6.3 Sense Field Selection

Each 16K word bit contains four sense windings, each of which senses 4096 cores. Each bit has an associated Type G022 Four Input Sense Amplifier. The outputs of the four amplified sections are gated on by four strobe pulses (CMSC STRB BIT 0-8, 9-17, 18-26, 27-PAR). A desired field is selected by enabling the field select gate for that amplifier section. The outputs of the four sections are ORed together to produce a common output pulse. The CMSC drawing shows the generation of the sense field selection pulses. A Type G023 Master Slice Control provides the discriminating level for all 37 G022 Sense Amplifiers.

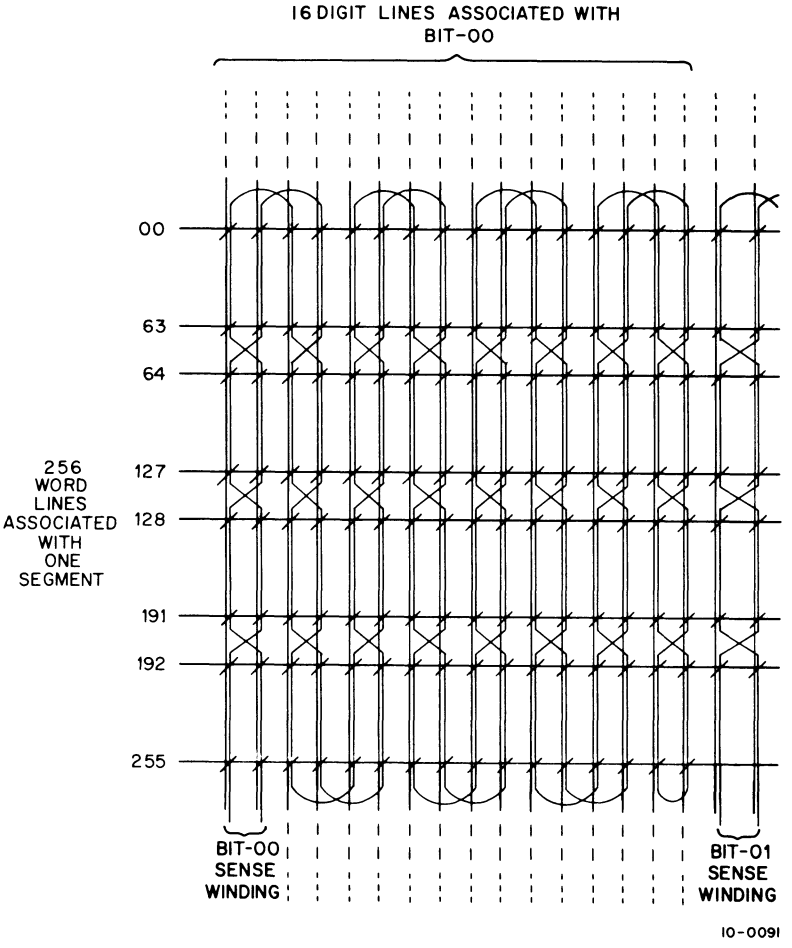


Figure 4-9 Sense Winding Configuration

CHAPTER 5
MAINTENANCE

5.1 SCOPE

This chapter describes the preventive and corrective maintenance procedures which apply to the MA10/MA10A Core Memories. Most memory maintenance procedures relate to the processor in use, therefore, all maintenance information applicable to the processor, including those documents listed under Reference Material in Chapter 1, must be available.

5.2 PREVENTIVE MAINTENANCE

A preventive maintenance program consists of the performance of specific tasks at intervals determined by the usage and down-time tolerance of the system. The benefit to be realized from a good preventive maintenance program is the discovery of conditions which, if ignored, might result in failure of the system at a later time.

All pertinent action taken during the performance of either preventive or corrective maintenance procedures should be entered in the maintenance log book.

5.2.1 Test Equipment

Table 5-1 contains a listing of test equipment required for performing the maintenance tasks. Table 5-2 contains the applicable diagnostic and test programs.

Table 5-1
Required Test Equipment

Equipment	Function
Voltmeter	Capable of measuring positive or negative dc potentials over a range of 0V to 70V with 3% accuracy.
Oscilloscope	Tektronix 453, or equivalent, calibrated against frequency and voltage standards.
ac Current Probe	Tektronix Type P6020 with terminator.

Table 5-2
Diagnostic and Test Programs

DEC Number	Name	DEC Number	Name
MAINDEC 10-D1An*	Simple Address Test	MAINDEC 10-D1Fn	User Mode BLT Test
MAINDEC 10-D1Bn	Micro Checkerboard	MAINDEC 10-D1Hn	PDP-10 Memory Test (Floating Zero/One)
MAINDEC 10-D1Dn	Checkerboard 2-1/2D	MAINDEC 10-D1In	Memory Heat Test
MAINDEC 10-D1En	Protection and Relocation Reliability	MAINDEC 10-D1Jn (Slow MA Setup)	PDP-10 Memory Test

5.2.2 Daily Tasks

Make a general visual inspection of the interior and exterior of the equipment. Correct obvious deficiencies such as burned out indicator lamps and improperly seated modules and connectors. Determine that fans are running and that air filters are not clogged with dirt.

5.2.3 Monthly Tasks

Run MAINDEC-10-D1Dn-PH (2-1/2D Checkerboard) taking voltage margins on sense amplifier thresholds. Log all margins on preventive maintenance voltage charts. Run DEC-10-D0Zn Timing Test (Speedy).

Clean all air filters.

5.2.4 Quarterly Tasks

Clean and inspect the interior and exterior of the equipment; repair all mechanical damage and replace any component or wiring which appears damaged or abnormal.

Margin the entire memory in accordance with Table 5-7. Log all margins on preventive maintenance voltage charts.

5.2.5 Power Supply Measurements

The Type 705 and 706 Power Supplies are shown in Figure 5-1 and 5-2, respectively. Also indicated on the figures are measuring points for each voltage. Table 5-3 lists the allowed tolerance and ripple content for each voltage.

*In all instances, use the latest available program version.

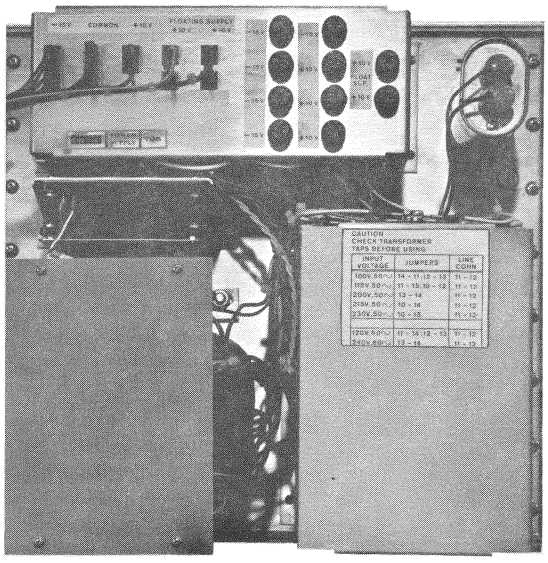


Figure 5-1 Type 705 Power Supply

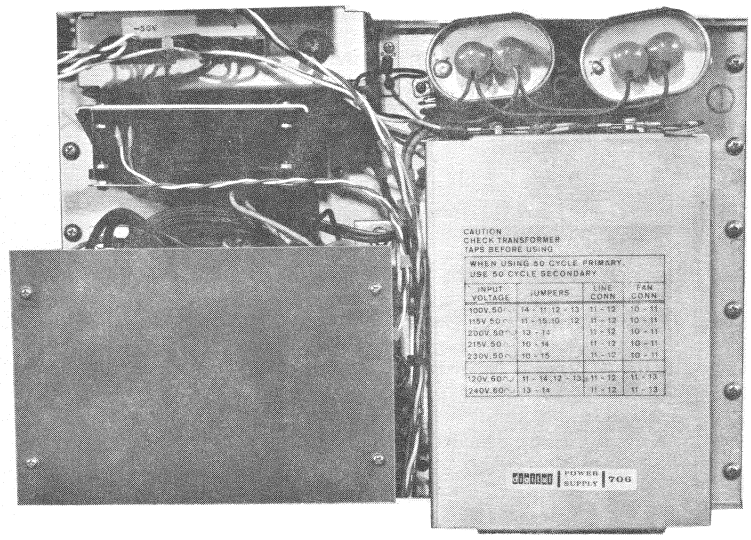


Figure 5-2 Type 706 Power Supply

Table 5-3
Power Supply Operating Specifications

Type 705			
Voltage	Tolerance	I max	Ripple max
+10V	9.4 to 11.0V	3.5A	300 mV
-15V	-14.5V to -16.0V	24A	700 mV
+10V (floating)	9.4V to 11.0V	4A	300 mV

Type 706			
Voltage		I load	Ripple max
Maximum	Minimum		
65V	49V	0.35A	Less than 1.5V
58V	49V	10A	Less than 1.5V
54V	49V	20A	Less than 1.5V

The output voltage must be within the values shown in Table 5-3 for all combinations of ± 15% line variation and ± 2% line frequency variation.

If the power supply potentials and/or ripple contents do not meet the specifications in Table 5-3, the power supply must be assumed to be defective. Under these conditions, the power supply must either be repaired or replaced since neither unit is provided with adjusting controls.

5.3 GENERAL MAINTENANCE

This section contains specific instructions concerning stack installation and checkout, margin testing, and troubleshooting.

5.3.1 Stack Installation and Checkout

At the time of uncrating, a careful visual inspection of the stack should be made to confirm the integrity of lines and solder connections, and the presence of the correct labels, fuses, etc. The following checkout procedure should be followed to ensure that the stack is in proper operating condition:

a. Check the low 8K W103 Card to determine that the thermistors are properly connected.

b. Correct any apparent deficiencies.

c. Plug in the stack and set up the drive currents, stagger delay, and strobe; refer to Tables 5-4, 5-5, and 5-6.

d. Drive current is measured from baseline to peak of BIT READ for address 000_8.

e. Stagger delay is measured from delay input to output (N40L to N40N).

f. Strobe is measured from the 10% point of the WORD READ drive waveform for address 000_8 to the 1.2V level of the CMSC STRB (00-08) pulse.

g. Deposit and examine all 1s and all 0s throughout the memory.

h. If bits are dropped or picked up, and the fault is found to be in the stack, determine the particular problem from Figure 5-3. Be precise as to the cause of the fault observed. If the fault is definitely in the stack, mask out the bad bits and proceed with Section 5.3.1 j.

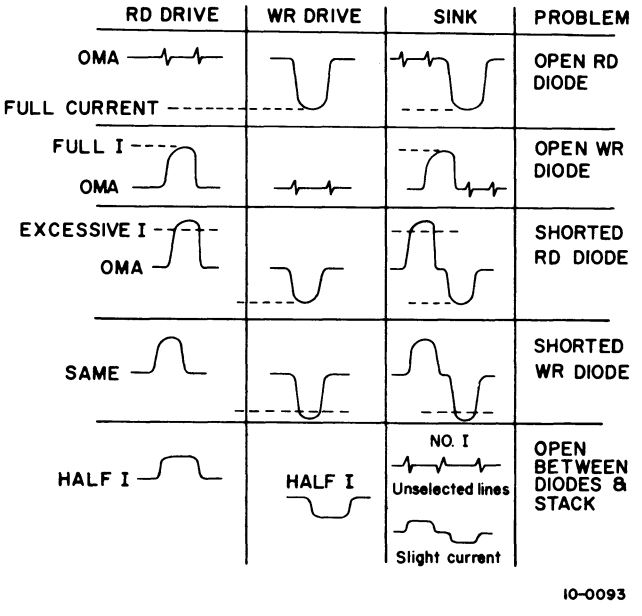


Figure 5-3 Stack Fault Indications

i. If no stack fault has been observed, run Checkerboard 2-1/2D, MAINDEC-10-D1Dn.

j. Measure the strobe in accordance with Section 5.3.1.1 and set the strobe to the center of the window.

k. Record the threshold margins and examine the bit or bits which exhibit low margins with the oscilloscope.

l. Record all low 1 addresses and the 1 output amplitude.

m. Vary the drive currents ± 5% and ± 10% and record the threshold margins and failing bits in each instance.

This procedure should determine the condition of the stack. If the stack meets the ±7V threshold margin specification, it is acceptable. If not, all faults must be clearly defined and the stack returned to the vendor or the nearest DEC Field Service Office, whichever procedure is appropriate for the particular installation.

Table 5-4
Stack Drive Current Requirements

Stack	Drive Current				
	-10%	-5%	Nominal	+5%	+10%
Fabritek	396 mA	418 mA	440 mA	462 mA	484 mA
EMI[1]	387 mA	408 mA	430 mA	452 mA	473 mA
Ferroxcube	450 mA	475 mA	500 mA	525 mA	550 mA

[1]EMI stacks bearing Serial Nos. 10001 through 10027 require the current values shown for the Fabritek stack.

Table 5-5
Preliminary Settings for Stack Testing
(Slice Level = 4.5V)

Stack	Drive[1] Current	Stagger Delay Ser. Nos. 3-57	Stagger Delay Ser. Nos. 1,2,60 up	Strobe
Fabritek	440 mA	100 ns	80 ns	130 ns
Ferroxcube	500 mA	90 ns	60 ns	145 ns
EMI	430 mA	100 ns	80 ns	130 ns

[1]The drive currents shown are for a temperature of 25°C (77°F). Note 1 to Table 5-4 also applies.

Table 5-6
Current Setup For Temperature Compensation

Approximate Room Temperature		Approximate Current (mA)			
°C	°F	Fabritek	EMI	EMI Ser. Nos. 10001-10027	Ferroxcube
35	95	427.50	417.50	427.50	487.50
30	86	433.75	423.75	433.75	493.75
25	77	440.00	430.00	440.00	500.00
20	68	446.25	436.25	446.25	506.25
15	59	452.50	442.50	452.50	512.50

Table 5-7
Margin Specifications

Diagnostic Program*	Special Instructions	Panels	Specification	
			±10V	-15V
MAINDEC-10-D1Dn-PH Checkerboard 2-1/2D	Starting Address 140 Data Switches 4 & 16 up	B	±7	±3
		C & D	+7.5 -5	±3
		A	±7.5	+3 -2.5
		E,L,S	±7.5	±3
		H,J,K	±7.5	±3
		F,P	+7.5 -4	±3
		M	+7.5 -4	±3
		N & T	±7.5	±3
		R	±7.5	±3
MAINDEC-10-D1Hn-PH Floating ZERO, ONE	PRF Testing; Run approximately 1 ms/RQ using repeat continue. Starting address 140_8; data switch 16 up.	N	±7.5	±3
		B	±7.0	NA
DEC-06M-691-RIM Pre 4 Auto BLT Trans. Test	Program in checkerboard mode. Data switch 8 up.	B	±7.0	NA

*When running programs, the KA10 PAR STOP Switch must be ON.

5.3.1.1 Strobe Window[1]

a. Set up the strobe in accordance with Table 5-5.
b. Run Checkerboard 2-1/2D and take threshold margins.
c. Turn the strobe delay out until an error is detected.
d. Record the relative position of the strobe.
e. Turn the strobe delay in until an error is detected.
f. Record the relative position of the strobe.
g. Compute the strobe window, and adjust the strobe delay to the center of the window.

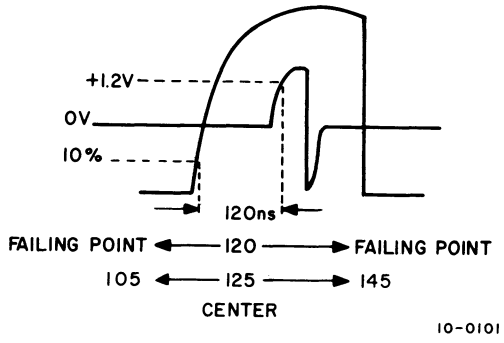


Figure 5-4 Strobe Window

[1]Before measuring the strobe window, the slice level must be adjusted to provide a symmetrical margin swing.

5.3.2 Timing and Power Shutdown Tests

5.3.2.1 Access and Acknowledge - Read access and write acknowledge times are measured at the processor including 10 ft of cable while running a repeat examine. Measure read access time between 2K01M and 2K01E; measure address acknowledge time between 2K01M and 2K01D.

5.3.2.2 Cycle Time - Cycle time (the period between Pn ACT going negative and CYC DONE(B) going negative) is measured at the memory. While running a repeat-examine, adjust the B312, T7 delay for a 930 ns cycle time.

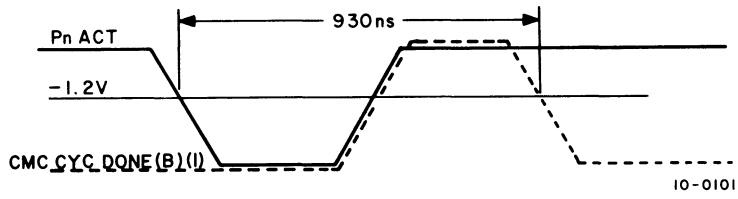


Figure 5-5 Cycle Time Measurement

5.3.2.3 Power Shutdown

a. The applicable program for this test is MAINDEC-10-D1Hn-PH (Floating ZERO/ONE).

b. Load the program in accordance with the instructions contained in the write-up.

c. The starting address is 140_8.

d. Set the address switches to 141_8.

e. With the MA10 Type 844 Power Supply control switch in the Remote position, turn off the processor power; the MA10 power should also go down.

f. Turn the processor power on.

g. Wait 10 seconds and depress Start.

h. The program should continue without error.

5.3.2.4 Processor Instruction Timing Test

a. The applicable program for this test is MAINDEC 10-D0Zn-PH, Processor Timing Test (Speedy).

b. The program should be run both with the FM enabled and disabled; interleaving is not specified; all instructions are in core; for those instructions with arguments, one argument is in core and the other in an AC; the tolerance is ± 5% of the nominal times shown in Table 5-8.

c. Memory cycle time is 1.0 μs and READ access is 0.55 μs.

Table 5-8
Processor Instruction Timing*
(Times shown are in microseconds)

Instruction	Fast ACs		~ Fast ACs	
	Nominal	5% High	Nominal	5% High
JRST	1.36	1.43	1.36	1.43
ADD	2.53	2.66	4.33	4.55
MUL (18 add/sub)	10.60	11.13	13.24	13.90
FAD (1 right-shift)	4.61	4.84	6.41	6.73
FAD (8 right - 3 left)	6.41	6.73	8.21	8.62
FMP (14 add/sub)	10.29	10.80	12.09	12.69

5.4 TROUBLESHOOTING

This section contains troubleshooting procedures arranged under "type of failure" headings. When attempting to isolate a fault, always take full advantage of the built-in maintenance aids, such as the MA10 and KA10 Indicator Panels and Switches.

5.4.1 Parity Errors

The Parity Stop switch on the KA10 console causes the computer to stop when a parity error is detected; the indicator panels display the register contents at the time of error detection. Observe the contents of the KA10 MA, AR, and Parity Registers and compare with the contents of the MA10 MA and MB Registers to isolate the fault.

If no errors are detected, deposit all 1s throughout the memory, and then run a Repeat-Examine with the Parity Stop switch ON. Repeat this procedure for a pattern of all 0s. Bits picked up or dropped and the failure addresses should be noted. The pattern of failures establishes whether the fault is due to a sense amplifier, a bit driver, or a word driver. If errors are still not detected, a quick repeat of the above procedures using +10V margins on Threshold, Sense Amplifiers, and MC10 Bus Transceivers should be tried.

Finally, the diagnostics; 2-1/2D Checkerboard, Floating ZERO and ONE, and other memory tests, Table 5-2, may be run. If necessary, margin the entire memory according to specifications, Table 5-7.

*Specifications are applicable to PDP-10 Systems only.

5.4.2 Control Logic Faults

In the event of a control problem, manifested by the INC indicator on the MA10 Indicator Panel, observe the state of the remaining indicators; i.e., RD RQ, and WR RQ. If the error can be caused by a Key Deposit or Key Examine, utilize the Repeat function of the KA10 to activate the memory control to allow observation with an oscilloscope.

If the failure is associated with the read-modify-write cycle, repeat execute a read-modify instruction from the console data switches.

Failure during the above procedures simplifies fault location within the control logic. Repetition rate sensitivity is determined by use of the console speed controls. The control logic may also be margined.

5.4.3 Multiple Memory Unit Selection Faults

This type of failure can be quickly isolated to the CMPC section of the logic; however, where more than one MA10 is installed within the system, an initial determination should be made that the fault is actually associated with a memory unit. This is accomplished by changing the MA10 switching addresses to several different configurations. Should the fault change location and more than one memory unit be affected, the fault is not associated with a memory unit. In this circumstance, a failing program should be run and a thorough oscilloscope investigation of the MA bus signals should be made. The most critical signals are the high order MAs; 22, 21, 20, etc. These signals should be observed with a dual-trace oscilloscope. Observe each with RQ CYC, noting any MA glitches during the period for which RQ CYC is true; this is the most critical time period.

5.4.4 Addressing Failures

This problem is indicated when two or more addresses are found to contain the same data (multiple addressing). Run a slow Repeat-Examine function while observing the MA indicators to detect any improper switching. If no error is indicated, run the Memory Address Test to isolate the fault.

5.4.5 Random Bit and Address Failures

Threshold maladjustment may be at fault. Run the 2-1/2D Checkerboard Test and test threshold and sense amplifier margins. Take a "Strobe Window" and reposition if necessary (Section 5.3.1.1). The window should be approximately 50 ns wide. When properly set, the leading edge occurs as the 1 read-out peaks; observation is made at the sense amplifier test points (pin J-low 8K; pin K-high 8K). Carefully observe the delta noise; the noise should not encroach into strobe time, if so, an increase in stagger-time delay (at N40) is probably necessary. A well tuned memory can exhibit ±9V margins on sense amplifier ±10V lines while running the 2-1/2D Checkerboard.

Other possible causes of failure in this catagory include:

a. A faulty G217 Memory Word Driver, if addresses of failures are associated with a series of word addresses.

b. A broken wire or poor contact at the Word Driver Connector (W012).

c. Open and/or shorted diodes in the stack word drive path.

5.4.6 Selection and Power Supply Failures

Because of the high currents utilized and critical power regulation requirements, this is probably the highest failure rate category in any memory system.

A faulty G805 Negative Regulator can cause failure of a G219 Memory Selector; therefore, when conditions such as a blown fuse or AW RQ failure are present, precautionary measures should be taken to prevent damage to replacement modules.

Following replacement of the blown fuse, and powering up, AW RQ should be true; if not, further investigation of the power supply is necessary (PSOK is probably not true). A second blown 25A fuse in the Type 706 Power Supply indicates trouble in the +V section of the power supply, one or more shorted G805 Regulators; one or more faulty G219 Drivers; or, a combination of the preceding.

Isolation of the fault is accomplished by shutting down power, removing all G805 Regulators and measuring the resistance to ground from the five output busses in the regulator section of Rack AB (-V and +V Busses). A short-circuit measured here isolates the problem to the G219s; no short-circuit, to the G805s. As the regulators are not now installed, they may be checked and any shorted or open transistors replaced. Depending upon the results of the resistance measurements, one of the two following troubleshooting procedures (a or b) should be used.

a. If no short circuit is measured, the G805s should be reinstalled two at a time, after being repaired where necessary. Begin at slots AB22 and AB20, because the G805 in AB22 supplies the base drive to the remaining ten regulators. Apply power and with a voltmeter measure the RD/WR potential between pin AK bus (-V) and pin BM bus (+V). This should measure approximately 32V. If the reading is normal, remove MA power with the REMOTE/LOCAL/OFF switch (wait 30 seconds for the power supplies to bleed) and install two more G805s. Apply power and perform the voltage measurement as previously described. Continue this procedure until the faulty G805 is located. Do not replace a G219 module until all G805s have been definitely determined to be operating properly.

b. If a short-circuit is measured, indicating that the problem lies with the G219s, perform the above measurements to ensure that the +V and -V voltages are normal before replacing faulty G219s; replacement is usually accomplished through a process of elimination.

Upon completion of the foregoing procedures, memory cycling should be attempted. Deposit all 0s in one address, then all 1s. If these tests are successful, deposit all 0s and all 1s throughout memory and proceed with the applicable diagnostics.

The G805 bases measured to ground from A20 should be approximately -1.5V. Nominal readings to ground for +V and -V are -20V and -60V, respectively. The +V potential is the variable and is dependent upon the type of stack installed.

CHAPTER 6
RECOMMENDED SPARE PARTS LIST

This section contains a listing of the modules (Table 6-1) and replaceable components (Table 6-2) used in the MA10/MA10A Core Memories with suggested spare quantities.

Table 6-1
Modules

DEC Type No.	No. In Use	Suggested Spares	DEC Type No.	No. In Use	Suggested Spares
B133	18	2	G217	16	2
B134	3	1	G022	37	3
B135	1	1	G219	74	3
B137	2	1	G626	4	1
B165	5	1	G700	11	1
B169	8	1	G703	4	1
B172	4	1	G704	31	1
B213	8	1	G805	13	2
B214	15	2	G816	1	1
B311	6	1	M502	4	1
B312	4	1	R303	3	1
B611	13	2	W102	11	2
B685	39	3	W501	1	1

Table 6-2
Component Parts

Item	DEC No.	Description	Suggested Spares
1	15-02762	3639B Transistor	10
2	15-03100	3009B Transistor	10
3	15-01742	2N 2904 Transistor	2
4	15-03099	2894-3B-S-Transistor	10
5	15-01881	2219-S-Trs-55	2
6	15-03399	3790-S	2
7	15-02155	1008-S	10
8	15-03409-01	6534 B	2
9	15-02762	3639	6
10	15-02937	3568	2
11	15-04809	2N 4234	2
12	15-03068	2N 315	2
13	15-02151	2N 3605	2
14	15-02762-01	3639C	6
15	11-00113	D662 Diode	10
16	11-00114	D664 Diode	10
17	11-03309	D671 Diode	2
18	11-03183	MR 2064	2
19	11-00118	1N 429 Diode	2
20	11-00123	1N 750 Diode	5
21	57-03408	-3V Strate	5
22	11-00106	Thyrector GE6RS20SP4B4	1
23	11-02942	1N 4001 Diode	1
24	11-05799	DM-15 Diode Pack	1
25	11-02933	DM-1 Diode Pack	1
26	15-09090-01	DEC-6B Transistor	6
27	19-09173-00	MC 1441 Int. Ckt.	4
28	15-05321	2N 4258 Transistor	10

APPENDIX A

GLOSSARY OF MNEMONICS

CMA	Core Memory Address This section of the logic appears on Drawing No. MA10-0-CMA and contains the CMA Buffer Register (MADR Bits 18-35) and the read and write request flip-flops.
CMA CLR	Core Memory Address Clear The pulse generated in the CMA after a processor request is received which clears the CMC control flip-flops and sets CMC RUN.
CMA RD RQ SEL	Core Memory Address Read Request Select The read level which initiates CMC timing pulses T1 through T4
CMA WR RQ SEL	Core Memory Address Write Request Select The write level which initiates CMC timing pulses T1 through T4.
CMAB	Core Memory Address Buffer This section of the logic appears on Drawing No. MA10-0-CMAB (2 sheets) and contains the CMAB buffers and the logic for generating CMAB WD WR (low 8K), CMAB WD WR (high 8K), and the CMAB MB CONTROL levels.
CMAB A CMAB B	Core Memory Address Buffer A and B Levels utilized in the CMDS logic for selecting digit lines.
CMAB MB CONTROL	Core Memory Address Buffer Memory Buffer Control Levels utilized in the CMAB for enabling the gates which generate the CMAB YMB levels.
CMAB WD WR (low 8K) CMAB WD WR (high 8K)	Core Memory Address Buffer Word Write Levels utilized in the CMWS logic for selecting word lines.
CMAB YMB 00-35	Core Memory Address Buffer Y-Dimension Memory Buffer Bits 00-35 Levels utilized in the CMDS logic for digit line selection.

CMAI	Core Memory Address Interface This section of the logic appears on Drawing No. MA10-0-CMAI and contains the signal terminations for the MADR lines.
CMB	Core Memory Buffer This section of the logic appears on Drawing No. MA10-0-CMB1-5 (5 sheets) and contains the buffering and gating for stack data input and output.
CMBI	Core Memory Buffer Interface This section of the logic appears on Drawing No. MA10-0-CMBI and contains the terminations for the core memory buffer lines.
CMC	Core Memory Control This section of the logic appears on Drawing No. MA10-0-CMC and contains the logic for generating the timing pulses; the read and write control levels; the START, SET, and RESET pulses; the CMB CLR pulses; and the error, run and done levels.
CMC BIT RD	Core Memory Control Bit Read The level which controls the turning on and off of bit read current.
CMC CMB CLR 1 and 2	Core of Memory Control Core Memory Buffer Clear 1 and 2 The pulses which clear the CMB, 216 ns after CMSC STROBE time, when in a write or read-modify-write cycle, and at T1 when in a read cycle.
CMC CYC DONE	Core Memory Control Cycle Done The level which is asserted at the completion of a memory cycle at time CMC T7.
CMC PROC RS	Core Memory Control Processor Restart The level which, with CMC PSE SYNC, allows generation of CMC T5 through T7 for completion of a clear-write or read-modify-write cycle.
CMC PSE SYNC	Core Memory Control Pause Sync The level necessary for generation of CMC T5 through T7 which cause write and completion of the memory cycle.
CMC RESET	Core Memory Control Reset The pulse which clears the CMC MB CONTROL and generates CMC STATE CLR and CMC SET.

CMC RESTART	Core Memory Control Restart The pulse generated by the momentary depression of the RESTART Switch initiating CMC START SET and RESET which ready the memory unit in anticipation of a request for access from a processor.
CMC SET	Core Memory Control Set The pulse which with CMC STOP (0) sets CMC CYC DONE and CMPC AW RQ, indicating to the processor that the memory unit is idle and available for access.
CMC START	Core Memory Control Start The pulse which clears CMC STOP and CMPC INCOMPLETE RQ during power-up conditions.
CMC STATE CLR	Core Memory Control State Clear The pulse which clears CMC CYC DONE, 116 ns prior to the setting of CMPC AW RQ during power-up conditions, and which clears the CMPC Pn ACT flip-flops.
CMC STOP	Core Memory Control Stop The level generated at time T5 when in SINGLE STEP and by CMC ERROR when the ERROR-STOP switch is on. This level prevents the setting of CMC CYC DONE and subsequent access.
CMC T1	Core Memory Control Timing Pulse 1 The pulse which causes bit read current to be turned on and clears the CMB in preparation for the reading in of data.
CMC T2	Core Memory Control Timing Pulse 2 The pulse which causes word read current to be turned on and initiates the strobe pulses.
CMC T3	Core Memory Control Timing Pulse 3 The pulse which causes bit and word currents to be turned off.
CMC T4	Core Memory Control Timing Pulse 4 The pulse which causes generation of CMC PSE SYNC if either or both of the CMA RQ flip-flops are set, thereby allowing CMC T5 to be generated.
CMC T5	Core Memory Control Timing Pulse 5 The pulse which causes write current to be turned on

CMC T6	Core Memory Control Timing Pulse 6 The pulse which causes write current to be turned off.
CMC T7	Core Memory Control Timing Pulse 7 The pulse which sets CMC CYC DONE at the completion of a memory cycle.
CMC WORD RD	Core Memory Control Word Read The level which controls the turning on and off of word read current.
CMC WR RS	Core Memory Control Write-Restart This pulse is initiated by Pn WR RS from the processor initiating the writing of a word into core when in a clear-write or read-modify-write cycle.
CMDS	Core Memory Digit Selection This logic appears on Drawing No. CMDS (19 sheets) and contains the logic for digit selection of data bits 00-35 and PAR.
CMI	Core Memory Indicators This information appears on Drawing No. MA10-0-CMI and contains the indicator lamp connections.
CMPC	Core Memory Processor Control This section of the logic appears on Drawing No. MA10-0-CMPC (2 sheets) and contains the logic for assigning and decoding the memory selection code, the priority logic, and the status flip-flops, CMPC AW RQ and CMPC INC RQ.
CMPC ACT STRB	Core Memory Processor Control Active Strobe The level which with CMPC Pn RQ (1) initiates the priority selection logic resulting in the setting of CMPC Pn ACT flip-flops.
CMPC AW RQ	Core Memory Processor Control Await Request The level which indicates that the memory unit is awaiting a request and which is required for granting access to a processor.
CMPC AW RQ (0)	Core Memory Processor Control Await Request The level whose positive-going transition generates CMA CLR.
CMPC INC RQ	Core Memory Processor Control Incomplete Request The level which enables the INC RQ indicator lamp indicating the

	occurrence of an error condition when CMC ERROR or CMC WR RS and CMA WR RQ (0) are asserted.
CMPC Pn ADDR ACK	Core Memory Processor Control Pn Address Acknowledge The pulse which is transmitted to the processor over an MADR line acknowledging a processor's request for access.
CMPC Pn MA SEL	Core Memory Processor Control Pn Memory Address Select The level which gates CMPC Pn ADDR ACK to the appropriate processor.
CMPC Pn MA STRB	Core Memory Processor Control Pn Memory Address Strobe The pulse which causes 1s on the MADR lines to be read into CMA 22-35 and the CMA RD RQ and CMA WR RQ flip-flops.
CMPC Pn MB SEL 1-4	Core Memory Processor Control Pn Memory Buffer Select The levels which control the setting of the memory buffer flip-flops.
CMPC Pn RD RS	Core Memory Processor Control Pn Read Restart The READ RESTART pulse which is transmitted to the processor over an MADR line indicating that there is data on the memory bus.
CMPC Pn REQ (1)	Core Memory Processor Control Pn Request The level which indicates that one or more of the CMPC Pn RQ flip-flops has been set by the enabling of a memory unit port selection gate. These levels generate CMPC ACT STRB.
CMPC P2 LAST	Core Memory Processor Control Port 2 Last Access The level which indicates that of P2 and P3, access has last been granted to P2.
CMPC P3 LAST	Core Memory Processor Control Port 3 Last Access The level which indicates that of P2 and P3, access has last been granted to P3.
CMPR	Core Memory Power Regulation This section of the logic appears on Drawing No. MA10-0-CMPR and contains the power regulation connections.
CMSA	Core Memory Sense Amplifiers This section of the logic appears on Drawing No. MA10-0-CMSA (2 sheets) and contains the logic for CMSA 00-35 and PAR.

CMSC	Core Memory Sense Control This section of the logic appears on Drawing No. MA10-0-CMSC and contains the logic for generating the CMSC STRB pulses and CMSC GATE levels for controlling the sense amplifiers.
CMWS (low 8K) and (high 8K)	Core Memory Word Selection Low or High 8K of Memory This section of the logic appears on Drawing No. MA10-0-CMWS and contains the logic for word line selection.
DSEL	Deselect Deselection of a processor at a port, accomplished by placing the 4-position wafer switch in the CMPC in the DES position.
~ FMC SEL	Not Fast Memory Control Select The level which is held at -3V for PDP-10 Systems (where the fast memory is contained in the processor).
INTL	Interleave The mode of operation whereby a pair of MA10s are accessed sequentially, odd addresses from one of the pair and even addresses from the other. This is accomplished by interchanging bits 21 and 35 of the address word.
MLBD	Magnetics Logic Block Diagram This information appears on Drawing No. MA-10-0-MLBD and contains a simplified block diagram of the READ and WRITE, FIELD and BIT selection systems.
Pn PARITY PULSE	Processor (n) Parity Pulse The PARITY pulse transmitted in both directions over an MADR line.
Pn REQ CYC	Processor Request Cycle The level transmitted to the memory unit over an MADR line which requests access to the memory and which remains until ADDR ACK is received by the processor.
Pn WR RS	Processor Write Restart The WRITE RESTART pulse transmitted to the memory unit from the processor over an MADR line when in a clear-write or read-modify-write cycle.
~ PSOK	Not Power Supply OK The level generated in the G816 Regulator Control which precludes memory unit operation during power up, down, and interrupt conditions.

APPENDIX B

LOGIC PECULIAR TO MA10 SERIAL NUMBERS 3-59

Certain logic operations are peculiar to MA10 units bearing Serial Numbers 3-59 inclusive, these operations are listed in this Appendix. Those engineering drawings which are applicable only to this serial number sequence are contained in Chapter 2, Volume II of this manual.

The switch panel applicable to Serial Numbers 3-59 is illustrated in Figure B-1. Although shown in four segments for convenience, the panel is actually one piece, mounted vertically on the right hand side of the logic wiring.

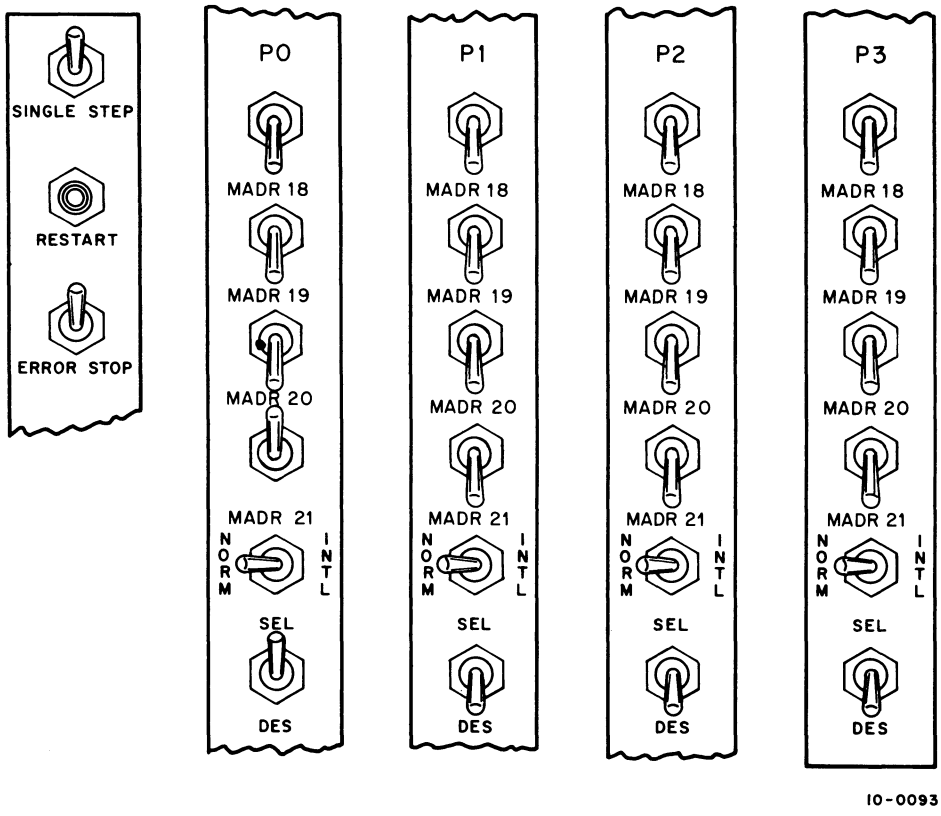


Figure B-1 Bracket Switch Panel

Logic peculiarities within MA10 equipment bearing Serial Numbers 3-59:

a. CMC START clears CMC PROC RS, CMC PARITY, and CMC PSE SYNC.

b. CMPC DELAYED T0 is generated 35 ns after CMPC T0 to clear CMPC AW RQ, CMC PSE SYNC, CMC PROC RS, and CMC STOP.

c. CMPC Pn IN is generated by Pn RQ CYC ANDed with the MADR bit 18-21 Switch outputs and ~Pn FMC SELECT, if the SEL/DES Switch is in the select position. CMPC Pn IN generates CMPC T0 which when ANDed with CMPC Pn IN sets one of the CMPC Pn RQ flip-flops.

d. Generation of the CMPC Pn MB SEL levels is dependent upon CMC CYC DONE B(1).

e. CMC CYC DONE B(1) OR CMPC Pn ACT(1) generates a CMPC Pn MA SEL 1,2, or 3 level.

f. CMC MA JAM 1 and CMC MA JAM 2 are generated by a CMPC Pn MA SEL 1 level.

g. CMC MA JAM 1 jams the content of MADR lines 22, 24, 26, 28, 30, 32, 34 and RD RQ into the MAR.

h. CMC MA JAM 2 initiates the CMC Timing pulses T1 through T4 and jams the content of MADR lines 23, 25, 27, 29, 31, 33, 35B, 21B, and WR RQ into the MAR.

i. The buffered CMC CYC DONE(1) levels, CMC CYC DONE B(1) and B(1)2, are generated.

APPENDIX C

CORE MEMORY FUNDAMENTALS

This discussion refers to the coincident-current ferrite core type of memory. From the hysteresis loop, Figure C-1, it can be seen that the core type under discussion exhibits a "square" characteristic. All reference to "points" in the following paragraphs refer to the hysteresis loop.

Assume that a core is threaded by an X and a Y line as in Figure C-2 (h). If the core is initially in the 0 state, applying half-select current in the write direction in either the X or Y line causes a flux change in the core corresponding to a move from the 0 state to point 1 on the loop. The core remains in this state as long as the drive current continues to flow. Upon interruption of current flow, the core moves back to the 0 state. The flux change associated with the move from the 0 state to point 1 is termed "reversible flux" as the core returns to its original state upon interruption of the drive current flow.

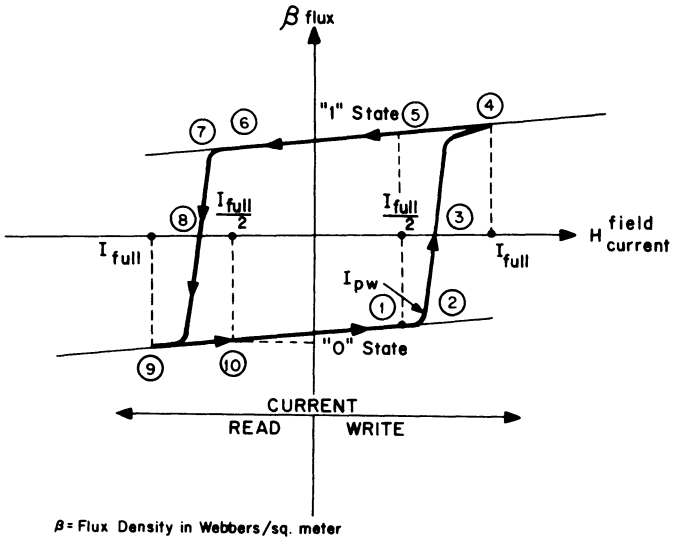


Figure C-1 Hysteresis Loop

When both X and Y half-select currents are flowing, the resultant current, I_{Full}, causes the core to move to point 4. The core remains in this condition until either the X or Y current is interrupted. If the current in one line is shut off, the core moves to point 5, while if the current in both lines is shut off, the core moves to the 1 state. In neither instance does the core move back to its original 0 state. The flux change associated with the move from the 0 state to point 4 is said, therefore, to be an irreversible flux change. The operations described in this and the preceding paragraph are the writing of a 1 and a 0 into a core, respectively.

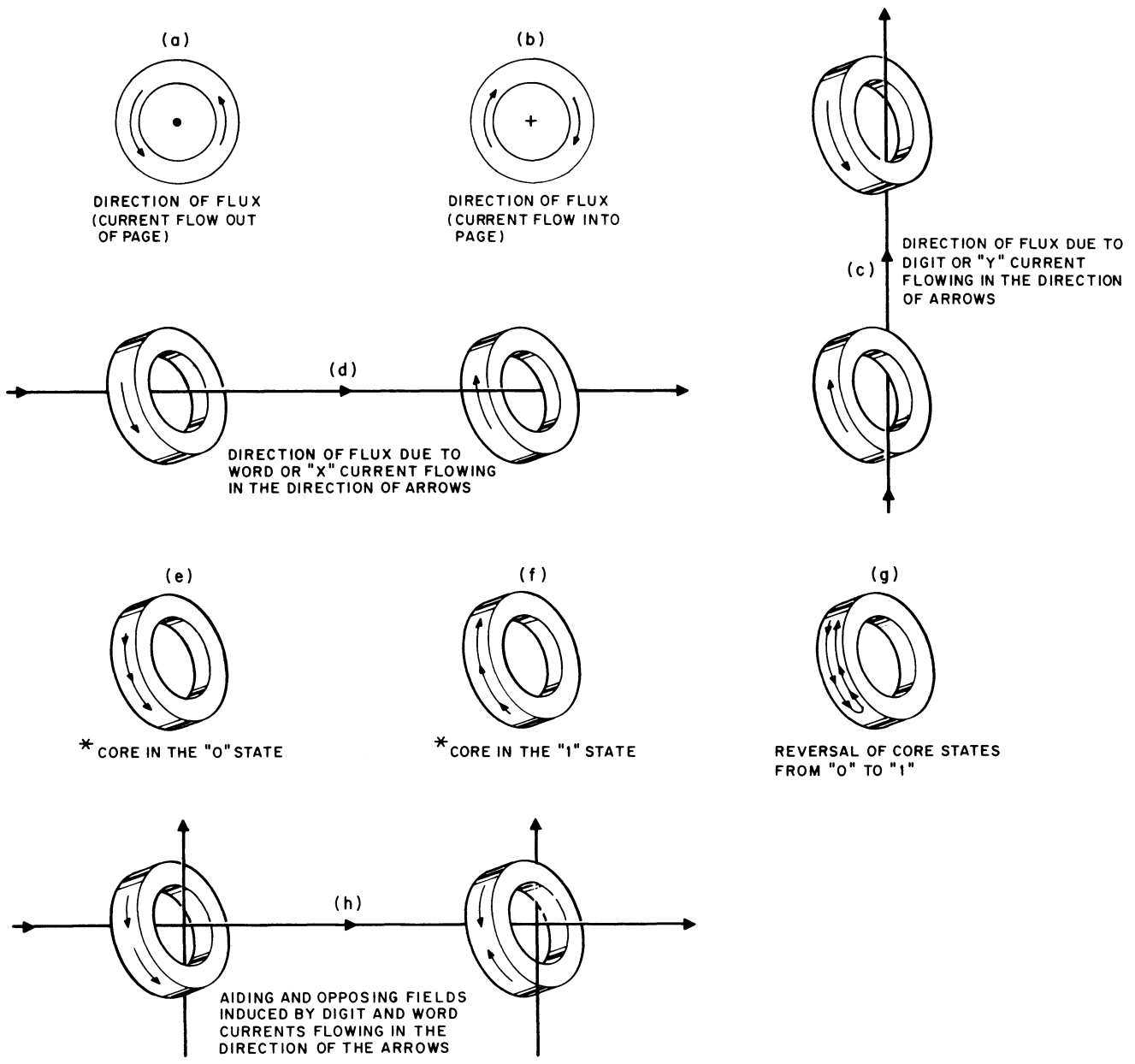


Figure C-2 Core Current and Field Relationships[1]

The point of non-reversible flux change (where when drive current is removed, a core goes to a state other than its original condition) is undefined but lies in the area of the "knee" between points 1 and 2. This point, designated I_{PW} ($I_{Partial\ Write}$), is dependent to some degree upon the period of time for which drive current

[1] The flux directions shown are obtained from the "Right Hand Rule"; i.e., if a current-carrying conductor is grasped by the right hand with the thumb extended parallel to the direction of current flow, then the fingers encircle the conductor in the direction of the flux.

flows. If the magnitude of drive current is greater than I_{PW}, the flux change is irreversible. Cores are not normally subjected to drive currents of magnitudes lying in the region between half-select and full-select, as the flux change places the core in a state which corresponds to neither a 0 or a 1; this is defined as "partial switching."

Although the discussion to this point has been concerned with writing into the core, and sense winding outputs have been of little interest, it should be noted that voltages are induced into the sense winding during the write operation. Figures C-3 and C-4 illustrate the sense winding potentials and currents. The first peak is associated with the movement from the 0 state to point 1. This is the reversible flux change region where peaks occur more rapidly than in the irreversible region. The maximum rate of flux change takes place at point 2 which corresponds to the point where maximum voltage is induced into the sense winding. At point 4 there is no longer any flux change, hence, no voltage is induced into the sense winding and the core is said to be "switched"*. As long as the drive current is sustained, the induced voltage remains zero. There is a negligible voltage induced into the sense winding when the current is removed and the core moves from point 4 to the 1 state.

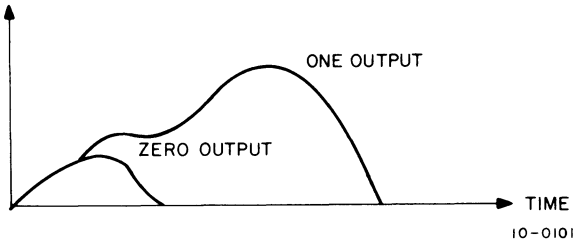


Figure C-3 Hypothetical Sense Winding Potentials

Reading of a 1 is accomplished by passing full read current through a core which is initially in its 1 state and sensing the change which takes place as the core moves to the 0 state. Potentials induced into the sense windings due to read currents are opposite in polarity to those which occur when the core is subjected to write current.

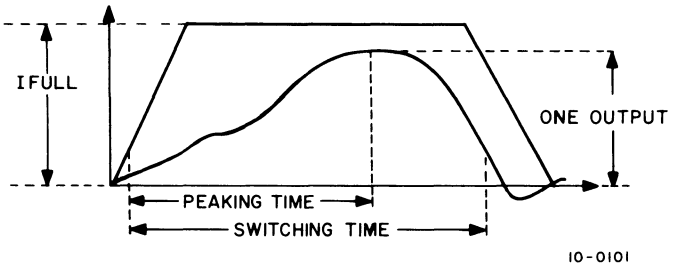


Figure C-4 Hypothetical Sense Winding Current

Assume that the core is initially in the 1 state as in Figure C-2(f). When half-read current is applied, the core moves out to position 6 causing a small flux change and inducing a correspondingly small voltage into the sense winding. Upon removal of the half-read current, the core moves back to the 1 state; the flux change has been in the reversible region. When full-read current is applied, the core moves to point 9 and, as it passes through the region of point 8 (maximum rate of flux change), a large voltage is induced into the sense winding. Shutting off current results in the core moving to the 0 state, inducing a small voltage into the sense winding. This is a read-destroy operation where the 1 content of the core has been sensed (read) and the core has been left containing a 0.

*Switching time is defined as the period between the 10% point of the drive current waveform's leading edge and the 10% point of the core output waveform's trailing edge.

When reading, the sense output winding is strobed or sampled at the point where the 1 output peaks, since the ratio of the 1 to 0 output amplitudes is greatest at this point. This point is defined as "strobe time".

If the core is originally in the 0 state and half-read current is applied, the core moves from the 0 state to point 10 and returns to the 0 state when the current is removed. If full-read current is applied to the core while it is in its 0 state, as in Figure C-5(a), the core moves out to point 9 and returns to the 0 state when the current is shut off. Both of these flux changes cause small voltages to be induced into the sense winding because the B/H loops are not perfectly square; i.e., a slight slope exists between 0 state and point 9. When in the 0 state and full-read current is applied, the core cannot move past point 9 because of the hysteresis nature of the core. Therefore, the core cannot be set to its 1 state by the application of read current. It can and will, however, change state from 1 to 0 when full read current is applied. The difference in amplitude between the voltages sensed when the core changes state from 1 to 0 and when it is in the 0 state and full-read current is applied provides the method for recovering the data stored in a core or an array of cores. The voltage induced into a sense winding from a core initially in the 1 state and pulsed with full-read current would appear as in Figure C-3.

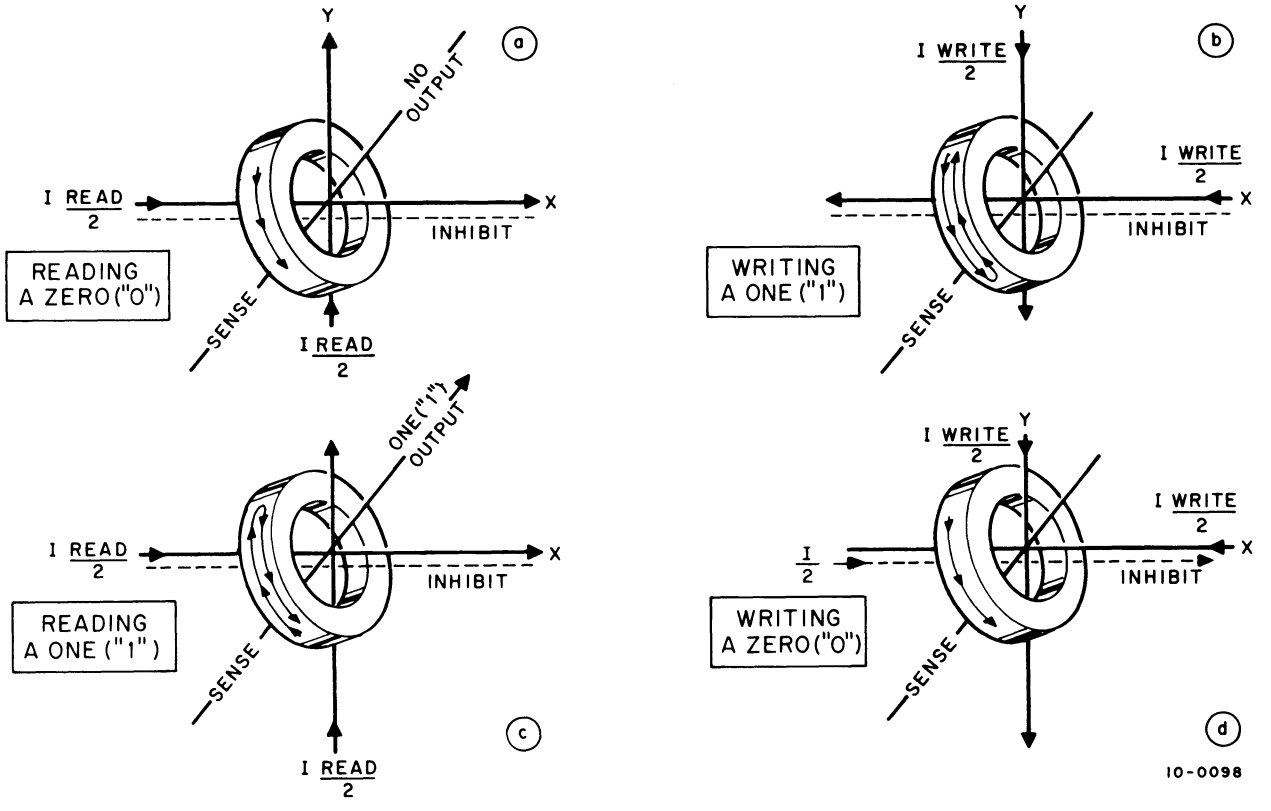


Figure C-5 3D 4-Wire Core States

A typical core array of coincident current memory is shown in Figure C-6. This array (64 x 64) contains 4096 cores. There are, therefore, 64 X and 64 Y drive lines which will carry the X and Y drive currents. Half-current is passed through each so that only the selected core is subjected to full-current. The remaining 63 cores on each axis are subjected only to half-select current and therefore do not change state. Current is passed through the cores in opposite directions for reading and writing and is controlled by switches which provide for selection of any one core within the array.

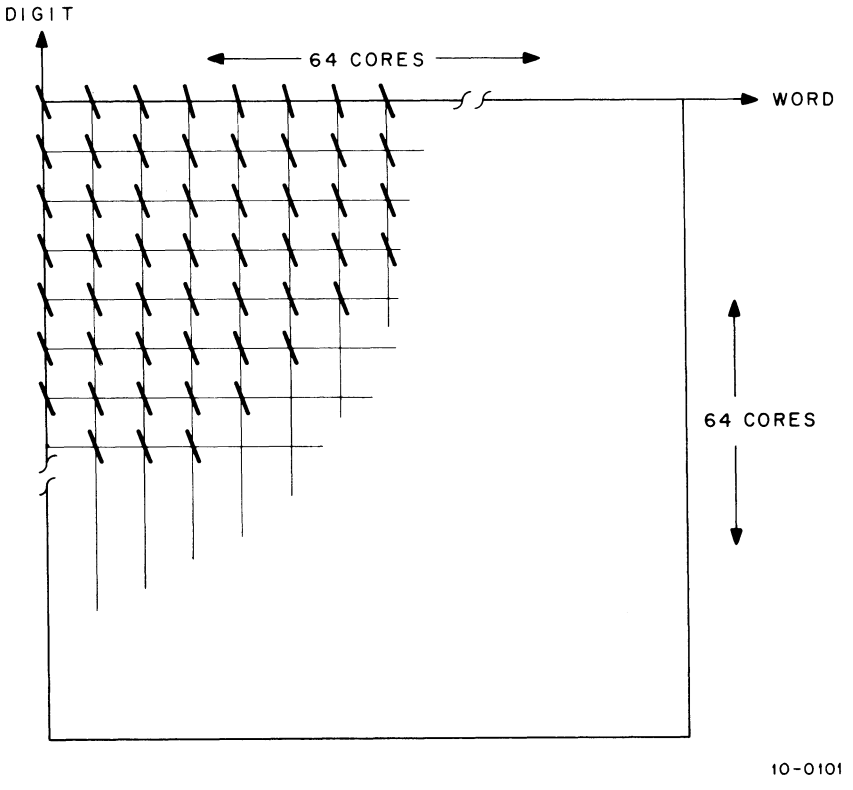


Figure C-6 64 x 64 Core Array

A sense winding is threaded through each core. When reading, the voltages sensed by the sense windings represent the data stored in the core (binary 1s or 0s). Differentiation between a 1 and a 0 is provided by the relative difference in the amplitude of the voltage sensed when the core is in the 1 state and is moved to the 0 state, or when in the 0 state initially and subjected to full-read current.

Writing of a 0 into a core (the core is initially in the 0 state as the memory location has been read and the contents destroyed prior to commencement of the write cycle) is accomplished by passing a resultant half-select current through the core, thereby not providing the requirement for a change of state. This situation is realized by the addition of a winding through the core in parallel with either the X or the Y line. This new line, called

the inhibit winding, is subjected to half-current in the direction opposite to the direction of flow of write current through the selected core when a 0 is to be written. The resultant current through the selected core, therefore, is (half write X + half write Y) - half inhibit; the selected core is subjected to only half-write current and no change of state takes place. The 3D 4-Wire Core States are illustrated in Figure C-5.

When it is desired to write a 1, inhibit current is not turned on, the core is subjected to full-select current, and a change of state from 0 to 1 takes place.

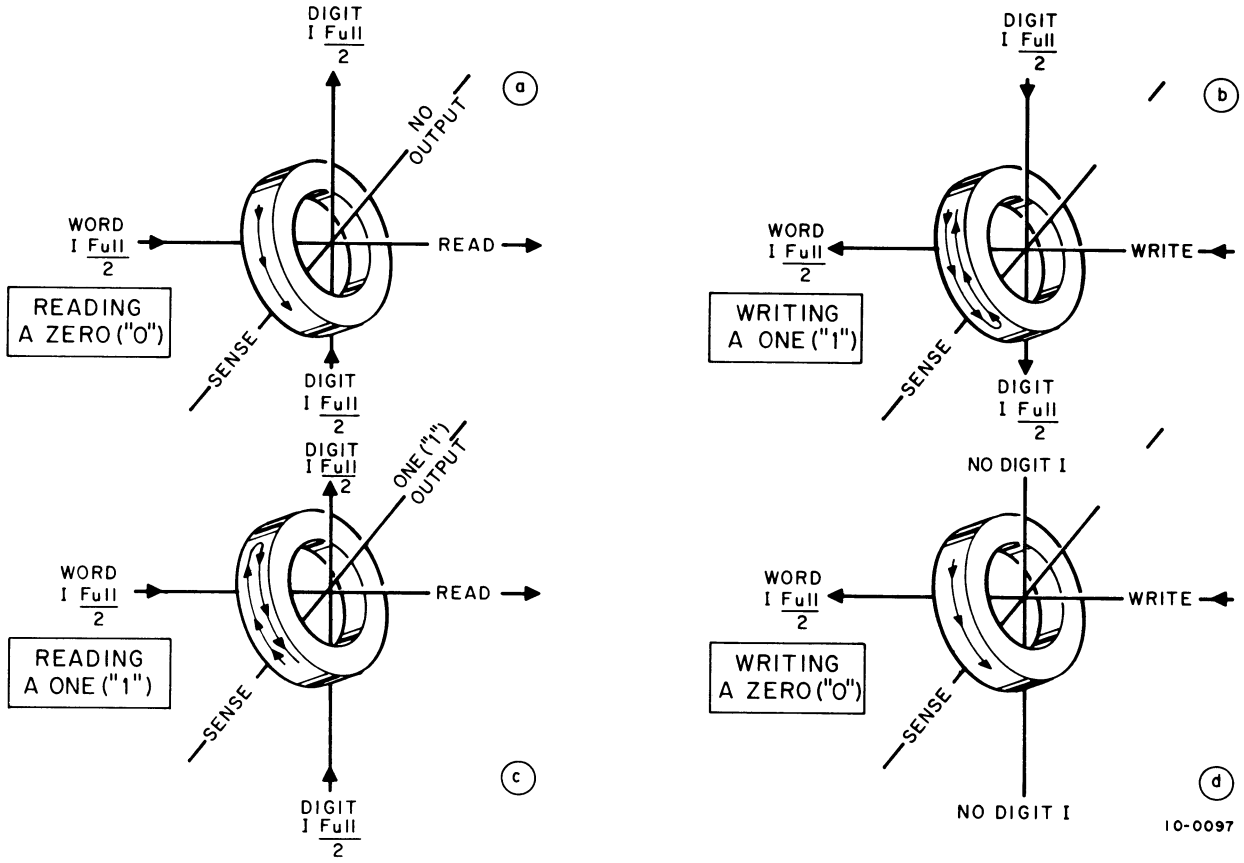


Figure C-7 2-1/2D 3 Wire Core States

In the 3D memory system, the cores associated with the bits of a word are distributed among as many arrays as there are bits in the word. A memory containing 18-bit words therefore requires 18 arrays. The X and Y lines are threaded in series through each array. The sense and inhibit wires are separately threaded through each plane with the inhibit wire running parallel to either the X or Y line. When half-select current is caused to flow in an X and Y line, one core in each array (each core representing one bit of the word) is subjected to full-select current. When reading, those cores which are in the 1 state induce a voltage into the sense winding associated with the array in which each 1 state core is located. Cores in the 0 state induce no voltage into

their associated sense windings. When writing, inhibit half-select current is turned on to the arrays associated with the bits where 0s are to be written; therefore, these cores are subjected to only half-select current and no change of state takes place. When writing 1s, inhibit current is not turned on.

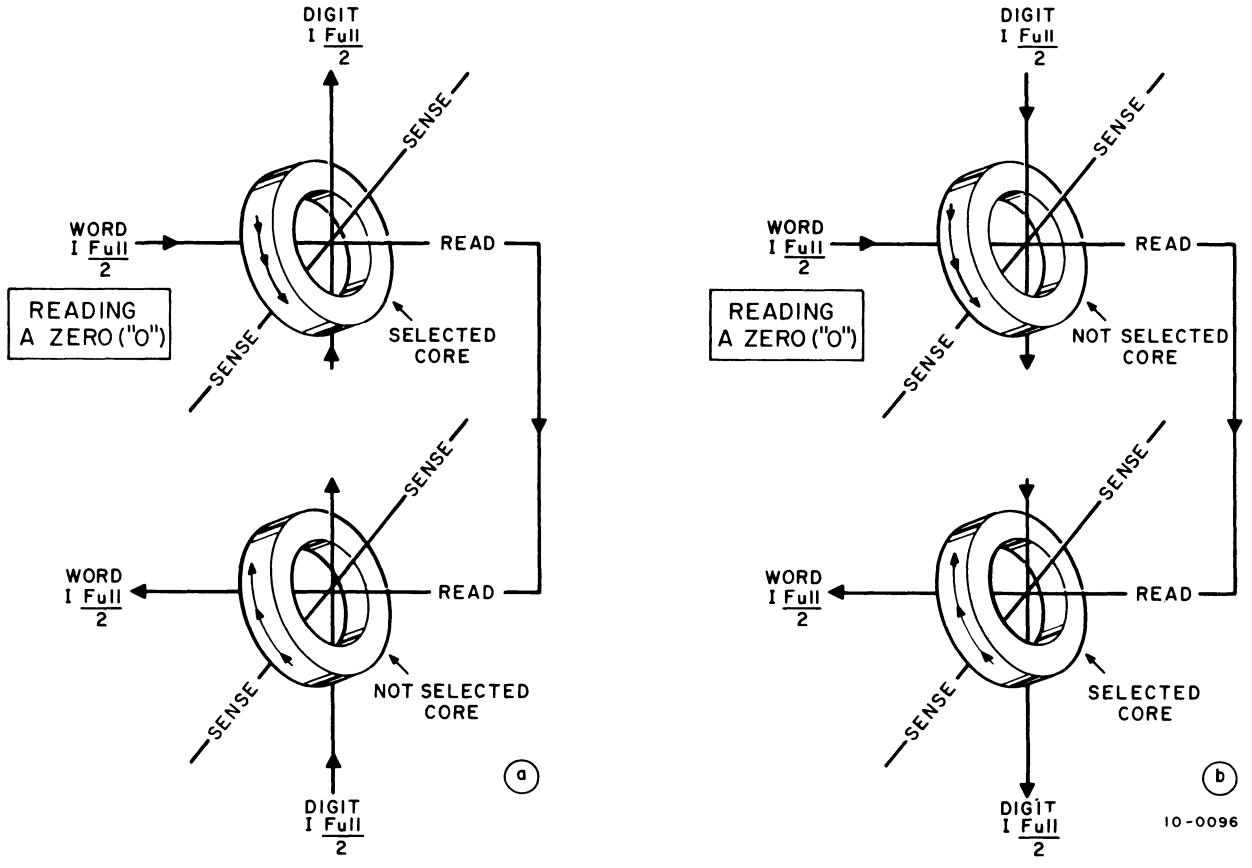


Figure C-8 Digit Line "Phasing" in the 2-1/2D System (READ Mode)

A 2-1/2D, 3-wire arrangement is used in the MA10. The planar arrangement of the stack is illustrated in Figure 4-6. In this system, 1 X-line and 36 Y-lines select a 36-bit word on one of four planes. The stack dimensions are commonly referred to as word and digit (or bit) dimensions rather than X or Y as in the 3D system. Both digit and word lines perform addressing functions while in a read cycle. When in a write cycle, however, digit lines perform the dual function of addressing and controlling the writing of data into the addressed location. When writing a 1, both word and digit half-select currents are turned on to the selected cores, causing a change of state from 0 to 1 as shown in Figure C-7(b). When writing a 0, however, (Figure C-7(d)) the core is subjected only to word half-select current. Current in the digit lines is controlled by the content of the data word to be written. When a data bit contains a 1, digit half-select current to the corresponding core locations is turned on; when the data bit is on a 0, digit current is inhibited to the corresponding cores and results in no changes of state.

There is, therefore, in the 2-1/2D system, no requirement for an inhibit winding; its function is performed by logic contained within the MA10 which turns digit current off and on depending upon the content of the data word to be written. The absence of the inhibit winding eliminates the noise coupled into the sense winding from the turn-off of inhibit current and enables the succeeding memory cycle to be initiated earlier, resulting in a faster cycle time.

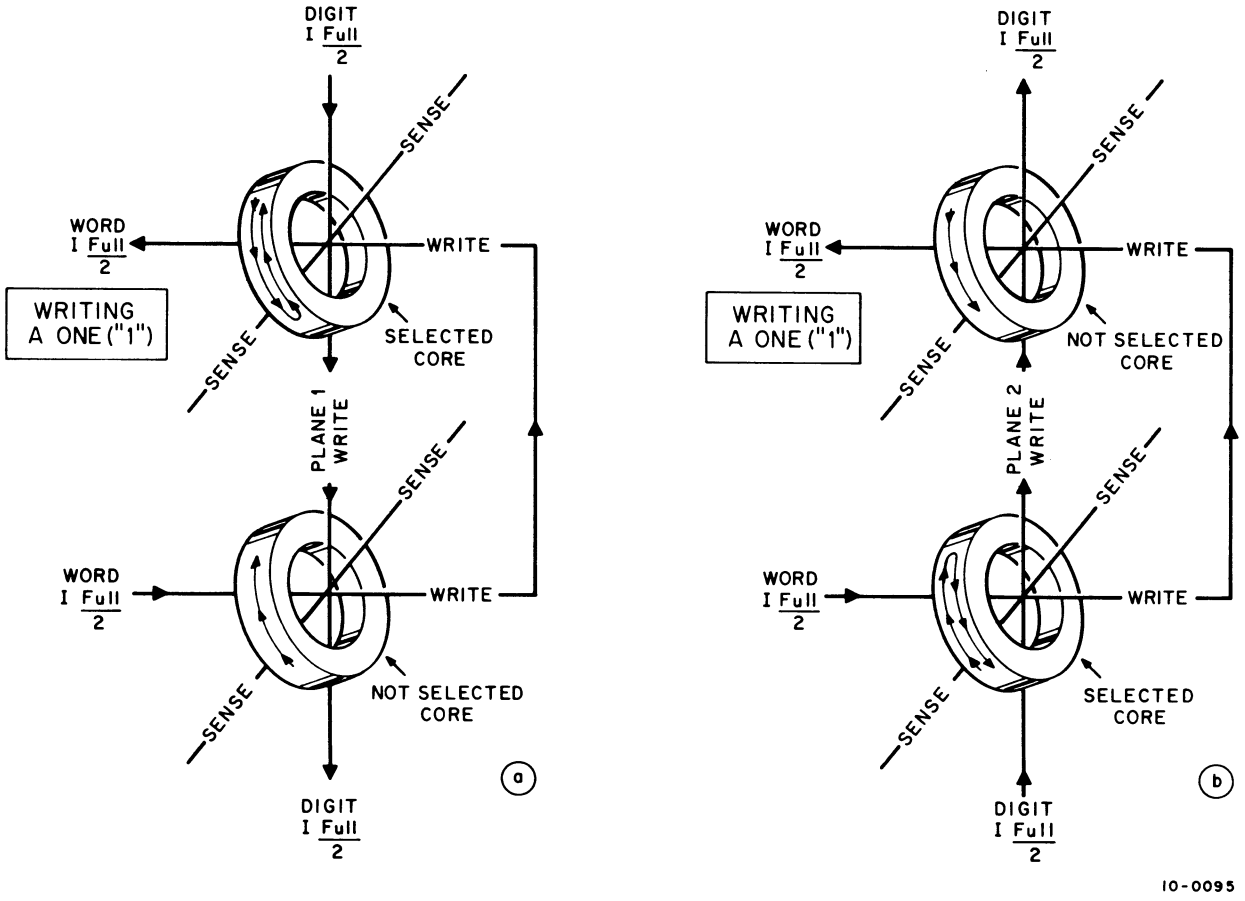
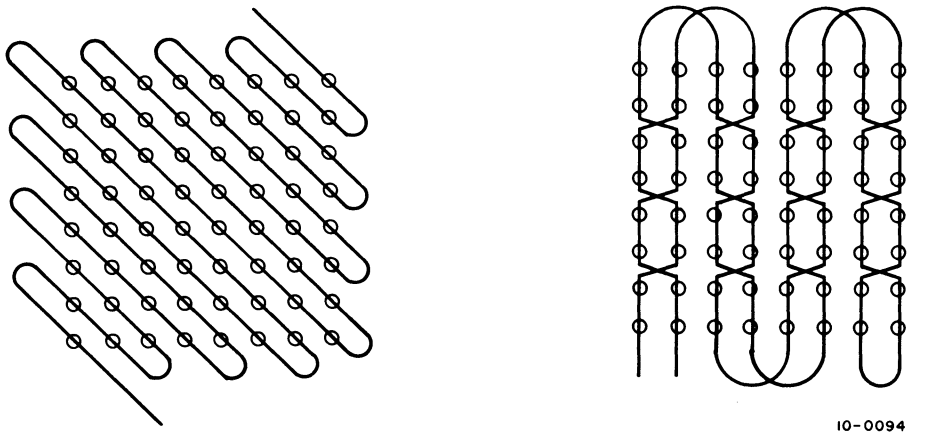


Figure C-9 Digit Line "Phasing" in the 2-1/2D System (WRITE Mode)

In the MA10, a technique called "phasing" is used to realize a 50% reduction in the number of required word line selection switches. Referring to Figure 4-5, it can be seen that for either the high or low 8K of memory, when a word and a digit line are pulsed, two cores are subjected to word and digit half-select currents. Figures C-8 and C-9 illustrate the phasing configuration. If it is desired to write a 1 into the core located on plane 1 (upper core in Figure C-9(a)), digit current would be caused to flow in the direction shown; the core is threaded in such a manner that the fields induced by word and digit half-select currents are aiding, and the core switches to the 1 state. In the lower core (located on Plane 2), however, the direction of current is such that the induced fields tend to cancel and no switching occurs because, due to the direction in which the word line threads

the core, the induced field (from the Right-Hand Rule) is in the direction opposite to the field caused by digit current. The hysterisis curve, Figure C-1, illustrates that the fields generated by read and write half-select currents are in opposition.

If it is desired that the lower core be selected, as in Figure C-9(b), digit current is reversed and a 1 is then written into the core located on plane 2. Selection between the two cores is accomplished by phasing (reversing) the direction of digit current for alternate planes in the stack.



(a)
Diagonal Sense Line Winding

(b)
Bow Tie Sense Line Winding

Figure C-10 Sense Winding Configuration

When one core of a 64 x 64 array is subjected to full current (selected), the remaining 63 cores threaded by these X and Y lines are half-disturbed (half-select current flows through them). As previously noted, half selecting a core causes a small output to be sensed by the sense winding. The 1 output of a core with an outside diameter of .022 in. might be on the order of 36 mV and the 0 output 2 mV. The polarity of the half-disturb outputs is dependent upon the initial states of the cores. If all of the 126 cores subjected to half-read current are in their 0 or 1 states, the voltage sensed will be of the same polarity and much greater in amplitude (126 x 2 mV = 252 mV) than a 1 output.

Therefore, a problem exists in choosing a configuration for the sense winding which will not allow the effects of the voltages sensed from the half-disturbed cores to be cumulative. A solution to the problem is to pass the sense wire through half the cores in one direction and through the remaining half in the opposite direction; this technique causes two voltages of opposite polarities to appear on the sense line with a resultant net effect of zero. Two methods of winding a sense line are illustrated in Figure C-10. The actual sense winding configuration used in the MA10 is the "Bow Tie". MA10 sense line selection is discussed in Section 4.6.

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